

NASA Report

167271
P-140

STUDY OF SWITCHING TRANSIENTS IN HIGH FREQUENCY CONVERTERS

**NASA Grant NAG 3-1236
Final Report**

*Department of Electrical Engineering
University of Akron
Akron, OH 44325-3904*

**Donald S. Zinger
Co-Principal Investigator**

**Malik E. Elbuluk
Co-Principal Investigator**

**Tony Lee
Research Assistant**

**Prepared For
NASA Lewis Research Center
Cleveland, OH 44135**

**Linda Burrows
NASA Project Manager**

(NASA-CR-193105) STUDY OF
SWITCHING TRANSIENTS IN HIGH
FREQUENCY CONVERTERS Final Report
(Akron Univ.) 140 p

N93-28327

Unclass

G3/33 0167271

ABSTRACT

As the semiconductor technologies progress rapidly, the power densities and switching frequencies of many power devices are improved. With the existing technology, high frequency power systems become possible. Use of such a system is advantageous in many aspects. A high frequency ac source is used as the direct input to an ac/ac pulse-density-modulation(PDM) converter. This converter is a new concept which employs zero voltage switching techniques. However, the development of this converter is still in its infancy stage. There are problems associated with this converter such as a high on-voltage drop, switching transients and zero-crossing detecting. Considering these problems, the switching speed and power handling capabilities of the MOS-Controlled Thyristor (MCT) makes the device the most promising candidate for this application.

This report gives a complete insight of component considerations for building an ac/ac PDM converter for a high frequency power system. A power device review is first presented in Chapter Two. The ac/ac PDM converter requires switches that can conduct bi-directional current and block bi-directional voltage. These bi-directional switches can be constructed using existing power devices. Different bi-directional switches for the converter are investigated Chapter Two.

Detailed experimental studies of the characteristics of the MCT under hard switching and zero-voltage switching are also presented in Chapter Three.

One disadvantage of an ac/ac converter is that turn-on and turn-off of the switches has to be completed instantaneously when the ac source is at zero voltage.

Otherwise shoot-through current or voltage spikes can occur which can be hazardous to the devices. In order for the devices to switch softly in the safe operating area even under non-ideal cases, a unique snubber circuit is used in each bi-directional switch. Detailed theory and experimental results for circuits using these snubbers are presented in Chapter Four.

In Chapter Five, a current regulated ac/ac PDM converter built using MCTs and IGBTs is evaluated.

ACKNOWLEDGEMENTS

We are grateful to the Power Technology Division at NASA Lewis Research Center for their support for this work. Special thanks to Linda Burrows for her cooperation throughout the project.

Special thanks to the Research and Development group of Harris Semiconductor™ Inc. for providing samples of MCTs used in the experiment work of the research.

TABLE OF CONTENTS

	Page
LIST OF TABLES	vi
LIST OF FIGURES	vii
 CHAPTER	
I. INTRODUCTION	1
Statement of The Goals	3
II. Switching Devices	7
2.1 Devices Overview	7
Power MOSFETs	7
Power Bipolar-Junction-Transistors (BJTs).	9
Thyristors	10
Insulated-Gate Transistors (IGTs)	12
2.2 The Mos-Controlled-Thyrsitor (MCT)	14
2.3 Bidrectional Switch Configurations	17
III. TESTING OF MOS-CONTROLLED THYRISTORS (MCTS)	24
3.1 Testing of MCT under hard switching	24
3.1.1 Procedure	24
3.1.2 Results and Comments	27
3.2 Testing of MCT under soft switching	32
3.2.1 The Block Diagram	32
3.2.2 The Zero Crossing Detector With Compensation	32
3.2.3 The Control Logic Circuit	33

CHAPTER	Page
3.2.4 Results And Discussions	34
IV. SNUBBER CIRCUITS FOR MCTS IN AN AC/AC PDM CONVERTER	45
4.1 Introduction	45
4.2 Snubber Circuits For Dc link Bi-Directional Switches	45
4.3 Snubber Circuit for Ac Link Bidirectional Switches	48
4.4 Experimental Results	67
Anode Kelvin Current	73
V. TESTING THE MCT IN A THREE PHASE CURRENT-REGULATED AC/AC PDM CONVERTER.	76
5.1 Introduction	76
5.2 Three Phase Ac Link PDM Converter	76
5.3 Current Regulated Ac/ac PDM Converter	80
5.3.1 Single phase current regulation	81
5.3.2 Three phase current regulation	87
5.4 The drive circuit	89
5.5 Experimental Results	89
VI. SUMMARY AND SUGGESTED FUTURE WORK	100
6.1 Summary	100
6.2 Suggested Future Work	102
BIBLIOGRAPHY	103
APPENDICES	104
APPENDIX I MCT DATA SHEET	105
APPENDIX II THE SCHEMATICS OF THE PDM CONTROL CIRCUIT	109
APPENDIX III ANALYSIS AND SIMULATION OF THE 20KHZ AC SOURCE – THE MAPHAM INVERTER	114

LIST OF TABLES

TABLE		Page
2.1	Summary of the Bidirectional switch configurations.	20
5.1.	A General Comparison Of PDM and PWM Technique	81

LIST OF FIGURES

FIGURE	Page
1.1	PDM ac motor drive with portability for different control schemes . . . 2
1.2	(a)Simplified single phase PDM circuit (b)Example of timing and control of switches and low frequency output voltage, Vout and current, Iout 3
1.3	Snubber capacitors used to prevent voltage spikes across the devices. . . 5
1.4	Snubber inductors in series with switches to limit shoot through current. 6
2.1	Circuit symbol for (a)N-type (b)P-type MOSFET 8
2.2	Circuit symbol for (a)NPN (b)PNP BJT 9
2.3	Using a Baker's Clamp Circuit to avoid hard saturation 11
2.4	Thyristor symbol and model 11
2.5	(a)The circuit symbol, (b) simplified Model and (c) structure of IGTs. . 14
2.6	(a)The circuit symbol, (b) the model and (c) the layout of an MCT . . . 16
2.7	Circuit symbol of a triac 18
2.8	Bidirectional switch configurations 19
2.9	Examples of power devices with built-in anti-parallel diodes 19
2.10	Three phase ac/ac PDM inverter using twelve MCTs. It requires the MCTs to be able to block voltage in both forward and reverse direction 21
2.11	Three phase ac/ac PDM inverter using twelve MCTs and twenty four diodes. They do not require the MCTs to have bidirectional voltage blocking capability. (a) Six isolated power supplies are needed but only six only drive circuits. (b) Needs five isolated power supplies but twelve gate drive circuits 23
3.1	A dc/dc down converter 25

FIGURE	Page
3.2 A single phase PDM converter	25
3.3 A simple push-pull gate drive circuit	26
3.4 Turn-off snubber connected in parallel with the diode to limit the dV_{AK}/dt when the MCT is turned off	27
3.5 Hard switching waveforms without snubber	29
3.6 Hardswitching waveforms with snubber	30
3.7 An improved gate drive circuit that can provide 200ns rise time	31
3.8 An RLC filter acts like a 4kHz current source load	35
3.9 Example timing and control of the switches	36
3.10 Block Diagram of the power circuit and its controller	36
3.11 Zero crossing detector that can detect before zero crossing	37
3.12 Illustration of the adjustable zero-crossing where V_n and V_p are the adjustable "zero-levels"; t_{cr} and t_{cf} are the positive- and negative-going zero-crossing compensations respectively	38
3.13 Timing diagram for the outputs of the ring counter and the control signals of S1 and S2	38
3.14 Karnaugh Map for the control signal of S1	39
3.15 Circuit that generates the control signal for S1 and S2	39
3.16 Voltage across the switches S1 and S2	40
3.17 Detail of voltage rise during turn-off	40
3.18 Detail of voltage across a conducting switch	41
3.19 Detail of current as S1 turns off and S2 turns on	41
3.20 Equivalent voltage across a bi-directional switch that is off	43
3.21 Waveforms of ac link voltage and voltage across each device in a bi-directional switch when off	43
4.1 A sketch of anode current I_A and anode-to-cathode voltage V_{AK} during turn-off with and without snubber circuits. And comparison of power losses	47

FIGURE		Page
4.2	A non-dissipative turn-off snubber circuit. This is supposed to connect in parallel with the free wheeling diode	48
4.3	An ac/ac PDM converter with simplified switches, S1 and S2 shown. Each switches consist of two MCTs and Two diodes	50
4.4	A turn-on delay of ΔT in S2 causes an instant of open circuit for the current source load. Two snubber capacitors are used to keep the current continue and reduce voltage spike across the devices	51
4.5	Graphical representation of ac link voltage, V_{ac} , and the voltage across each switch during ΔT	53
4.6	Ordinary turn-off snubbers used in a Bidirectional switch	54
4.7	An PDM converter with a Mapham inverter as a voltage source	55
4.8	An example waveforms of voltages across the ac link and the switches during an instant of short-circuit across the ac source.	55
4.9	A turn-off delay of ΔT in S1 causes an instant of short circuit for the voltage source. Two snubber inductors are used to limit the shoot through current	57
4.10	For small ΔT the area under the sinewave can be approximated by a triangle	57
4.11	The best location of the snubber inductor and free wheeling diode in each bidirectional switch	58
4.12	Proposed snubber for the by directional switch which combines the features of both capacitive and inductive snubbers	60
4.13	Simplified ac/ac PDM converter with proposed snubber circuit. Each snubber inductor has a free wheeling diode (not shown) in parallel with so that no voltage spike across the devices at turn-off	60
4.14	Voltage and current responds as a current step inputs to a parallel LC and diode circuit	62
4.15	Voltage and current responds as a current step inputs to a parallel LC and diode circuit with the switch has a turn-on delay of ΔT	64
4.16	B-H curve for a saturable inductor	66

FIGURE		Page
4.17	An ac/ac converter With Proposed snubber Circuit	67
4.18	Voltage across anode to cathode and cathode current of M11 without snubber	69
4.19	Voltage across anode to cathode and cathode current of M11 with capacitive snubber	70
4.20	Voltage across anode to cathode and cathode current of M11 with inductive snubber	71
4.21	Voltage across anode to cathode and cathode current of M11 with both capacitive and inductive snubber	72
4.22	Output voltage and load current with proposed snubber	73
4.23	The MCT pinout and symbol	74
4.24	(a) Anode Kelvin Current I_{KEL1} of M1, (b) Cathode current of M11 . .	75
5.1	Demonstration of (a) single (b) three phase ac/ac converters	77
5.2	(a) Example of maximum possible fundamenta, line-to-common, Vao, and line-to-line voltages, Vba.(b) maximum possible equivalent line-to-line voltage	79
5.3	Implementation of a Bidirectional switch for (a) ac link converters (b) dc link inverters	79
5.4	Current regulation of a single phase PDM converter using a two state comparator	82
5.5	Current regulation of a single phase PDM converter using a three state comparator	83
5.6	Single-phase current regulated PDM converter to be simulated	84
5.7	Simulations of Output Voltage and Current using two-state switching	85
5.8	Simulation of Output Current and Voltage using three state switching, zero-state is chosen when error current e_{ia} is within 3% of the peak command current	86
5.9	(a) Implementation of a three phase current regulated ac/ac PDM converter. (b) the three phase PDM bridge	88
5.10	The MCT and IGBT drive circuit used in the ac/ac PDM experiment . . .	89

FIGURE		Page
5.11	(a) line-to-common voltage, (b) details of , V_{co} , (c) line current, I_c	91
5.12	(a)Details of voltage across a switch made of IGBTs, (b)current through the switch	92
5.13	(a) Voltage across the MCT of a bi-directional switch, (b) collector current through the MCT, (c) product of (a)&(b); instantaneous power	93
5.14	(a) Details of voltage across an individual MCT, (b) current through the MCT	94
5.15	(a)Details of voltage across a switch made of MCTs, (b) current through the switch	95
5.16	The line-to-line voltage, V_{bc}	95
5.17	The ac/ac PDM converter with a modified starting sequence	99
A1.1	Manufacturer's Test circuit for MCTA75P60	107
A2.1	Zero-crossing switching control circuit	110
A2.2	The triangle wave generator that provides "TRI"	111
A2.3	Current limit signal, LMT, generator	112
A2.4	Cable pinout	113
A3.1	Using a synchronous generator to generate ac voltage	115
A3.2	Using a Mapham (resonant) inverter to generate ac voltage	116
A3.3	Idealized waveforms of currents and voltage of a Mapham inverter in steady state under no load	118
A3.4	The simulation of a Mapham inverter with a 4 Ω load connected.	120
A3.5	The simulation of a Mapham inverter with a 10 Ω load connected.	121
A3.6	The output voltage regulations at different loads.	121
A3.7	A Mapham inverter loaded by a ac/ac PDM converter.	122
A3.8	Simulation of A Mapham inverter loaded by an ac/ac PDM converter.	124

FIGURE	Page
A3.9	A simulation result with L_r and C_r equal to $6\mu\text{H}$, $6\mu\text{F}$ 125
A3.10	A Mapham Inverter loaded by a full-wave rectifier 126
A3.11	The current of the resonant inductor, L_r , and output voltage of the Mapham inverter shown in Fig. A3.10 126
A3.12	The output current, I_o , of the Mapham inverter in Fig. A3.10 127

CHAPTER I

INTRODUCTION

Since solid state devices has been introduced to industry, the controls of power conversions, by means of power electronics, has become simpler and more efficient. Recent work has suggested the use of 20kHz ac link for space station power distribution [1,2]. With today's technology, the reduced size and mass of high frequency power electronic circuits has made the 20kHz voltage source in space station possible. Although power electronics technology is characterized by high power density and efficiency, there are still problems such as switching transients, losses and stresses on the semiconductors. Thus, the reliability of power converters and voltage sources at space application is questioned. The objectives of this study are to minimize the effects of these problems.

Ac/ac conversion is the main stream of this report because of the advantages of using high frequency ac link. The technique of pulse density modulation (PDM) is used. A converter using the technique work off either an ac or dc voltage source. If a dc source is used, it involves quasi-resonance [3] which, however, will not be discussed in this report. An ac/ac PDM converter is a power converter using this new modulation technique to synthesis low frequency voltage and current. It takes the advantage of switching the devices at zero voltage crossing which minimizes switching losses. In order to guarantee switching at zero voltage, fast switching devices are required in PDM converters. Unfortunately, most switching devices trade off between speed and electrical

ratings (e.g. maximum blocking voltage and maximum conducting current). Therefore selection of switching devices is a main concern.

In most applications, mechanical power is the ultimate output therefore electric motors are needed. Dc motors have been used because of the simplicity of their control or if an ac source is not available, however, the expense of their high maintenance cost is generally high. Ac motors, on the other hand, are rugged and have low maintenance cost, and such features are especially important in space application. Advanced research has made ac motors an alternative to dc motors. With today's technology, availability of reliable ac source for space station is possible. Moreover, many control schemes for induction motors such as field oriented control and direct self control [4] have shown fast torque response.

Although control of ac motors will not be discussed in detail in this report, a "portable" PDM ac motor drive shown in Fig. 1.1, will be presented. Command currents i_{as}^* , i_{bs}^* and i_{cs}^* are obtainable from most control methods like field oriented control. Thus the PDM ac motor drive can become part of any control loop.

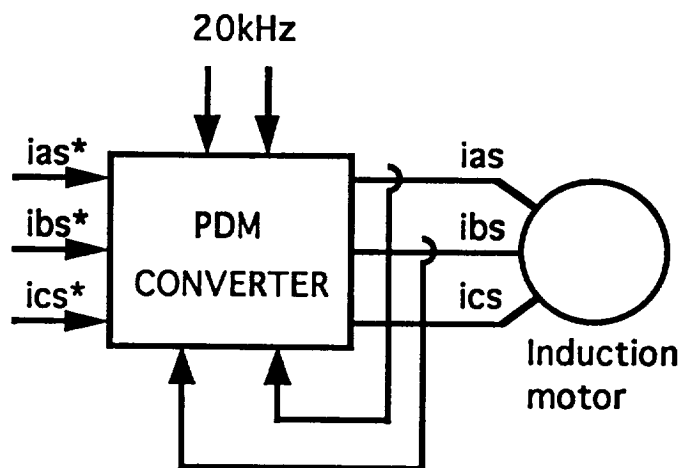


Fig. 1.1 PDM ac motor drive with portability for different control schemes.

The simplified single phase PDM circuit is shown in Fig. 1.2(a), which is just one third of the PDM converter shown in Fig. 1.1. A low frequency output of 4kHz is used as an example. In practical applications, output frequencies are a lot smaller compared to the ac link making the high frequency component easily filtered.

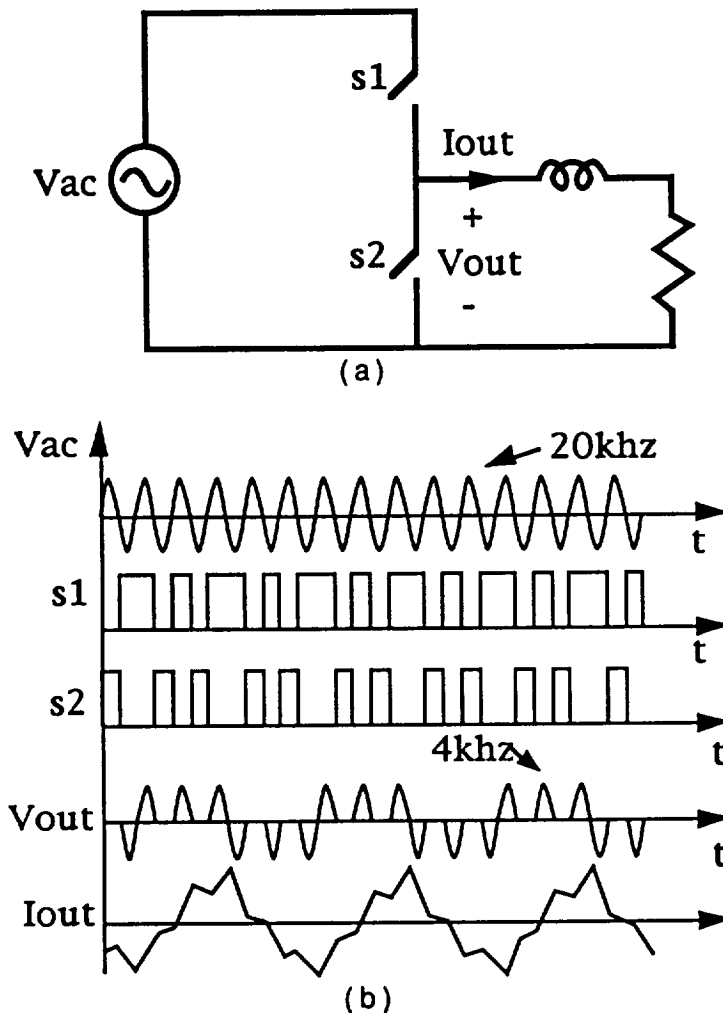


Fig. 1.2(a) Simplified single phase PDM circuit. (b) Example of timing and control of switches and low frequency output voltage, V_{out} and current, I_{out} .

Statement of The Goals

Power electronic technology is characterized by higher efficiency, lighter weight and higher power density compared to traditional power conversion technology,

In spite of the many advantages of power electronic circuits a major portion of the converted power is losses in the switching and conduction losses of the switching device.

Basically, to minimize switching losses, the switching devices should be switched at either small voltage or small current. This can be achieved by switching the device at zero-crossing of the ac input source voltage. A pulse density modulation (PDM) converter, for example, minimizes the switching losses with zero-crossing switching technique. However, there are problems associated with this converter such as the requirements of fast switching devices and ability to turn-on at zero volts.

Conduction losses can be minimized by choosing low forward voltage devices. However, the existing devices are either fast switching or low forward voltage but not both. It seems no power device is the best for a PDM converter. This report will address the issues of switching and conduction losses and give direction to selection the switching device in ac/ac PDM converters.

Switching at or near the zero crossing of high frequency link can reduce switching losses to a minimum. However, an inductive load forces the low frequency output current to be continuous, as shown in Fig. 1.2, and in such cases the load can be modeled as a low frequency current source. Both the switches s_1 and s_2 should not be opened at any moment, otherwise the load current source would be interrupted and large voltage spikes would be induced across s_1 and s_2 and may exceed the breakdown limits of the switches. If both the switches are closed at the same time, they short the voltage source and cause current shoot through which can exceed the current rating of the switching devices. This requires extremely tight timing for the switches compared to the conventional PWM inverter which has a freewheeling diode at each switch. Previously this problem was avoided by delaying turn-on of the incoming switch and adding a snubber capacitor across each switch as shown in Fig. 1.3. Although the rate of change of voltage across s_1 and s_2 is limited, the voltage held by the capacitors is discharged

through the switches at turn-on. Shorting the capacitors before the devices are fully turned on causes significant power dissipation in the devices. As a dual of the snubber mentioned above, an inductor can be placed in series with each switch as shown in Fig. 1.4. In this circuit the turn-on of the incoming switch is advanced and the inductor prevents the device from having an excessive shoot-through current. Unfortunately, current in the snubber inductors is bi-directional, and a free-wheeling diode cannot be connected in parallel with the inductors in order to avoid large induced voltage at turn-off. Both the snubber circuits discussed above cause problems at either turn-on or turn-off. Therefore there is a need to search for better and improved snubber circuits. This issue is addressed in this report.

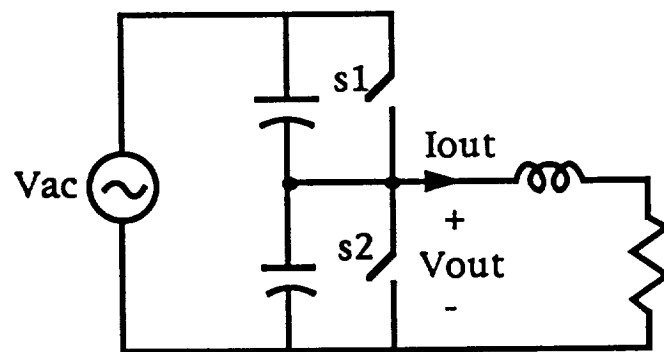


Fig. 1.3 Capacitors used as snubber to prevent voltage spikes across the devices

Fully controlled power devices, like BJTs and MOSFETs, do not have bi-directional voltage-blocking capability. Therefore fully controlled bi-directional switches are made up by combining diodes with the controlled devices. There are different configurations of such bi-directional switches. However, the advantages and disadvantages of these configurations are not fully investigated. In this report an attempt is made to characterize the trade-offs involved in choosing bi-directional switches.

The MOS-controlled-thyrister (MCT) emerging as a new power device that combines power density, low losses and fast switching device which may make the best candidate for PDM converters. However, it has been reported that this device is unable to turn on at zero voltage and considered not suitable for PDM converter [5]. This report gives a better understanding and solve the problem of zero voltage switching.

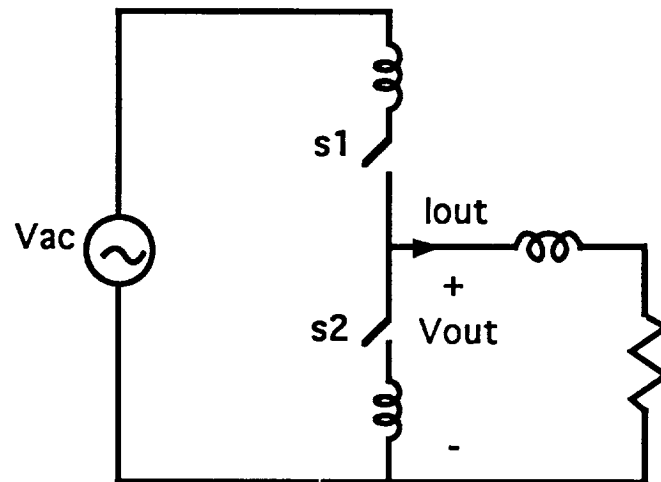


Fig. 1.4 Snubber inductors in series with switches to limit shoot through current

CHAPTER II

SWITCHING DEVICES

The selection of power devices for power converters is based on speed, capability of switching at zero voltage, loss and power density. Loss and power density are especially important if an expensive electrical power such as by space power, which is estimated to be more than \$500/kWh to be generated [1]. There are trade-offs between switching speed, ratings and losses. In the following section, the some major power devices will be reviewed and compared briefly. The newly emerging devices such as IGTs and MCTs will also be introduced.

2.1 DEVICES OVERVIEW

Metal-oxide-semiconductor field effect transistors (MOSFETs) and bipolar junction transistors (BJTs) are the major categories of fully controlled power devices. Although they have been used in power circuits extensively, when it comes to an ac/ac PDM converter for space power applications, the switching speed of the BJTs and the ratings of the MOSFETs become questionable. To improve upon these devices a hybrid device , the insulated-gate-transistor (IGT), was developed that obtains the switching characteristics of a MOSFET and the current density of a BJT. These power devices will be briefly discussed in the context of their application in ac/ac converters.

Power MOSFETs

A Power MOSFET, shown in Fig. 2.1, is a majority carrier switching device. Majority carrying devices are faster because minority carriers do not need to be

injected or removed from the device. It is controlled by its gate voltage, rather than current, therefore requiring a simpler gate drive circuit.

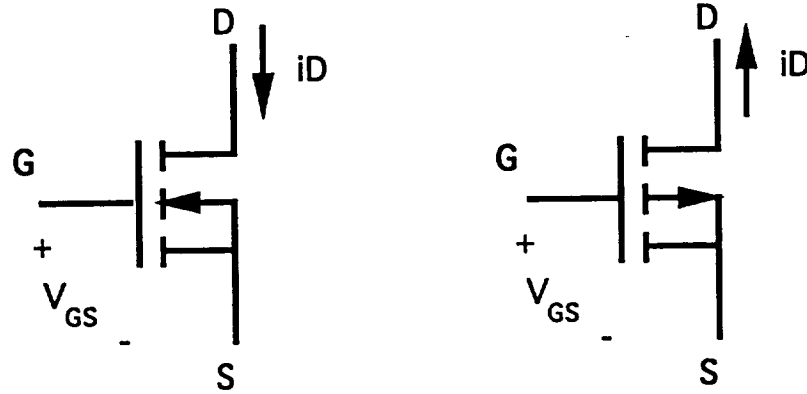


Fig. 2.1 Circuit symbol for (a) N-type, (b) P-type MOSFET

When on, the device looks like a resistor of value R_{on} which consists of two parts. The first part is called channel resistance which, also, exists in all signal level MOSFETs. The second part is the extended drain resistance which is unique to power MOSFETs. Extended drain region is needed for sustaining high voltage, usually above 100V, and the higher the voltage rating the longer the extended drain region. Since extended drain is lightly doped it constitutes a higher resistance and dominates the resistance of the device. This resistance is represented by (2.1) [6], where V_{BR} is the reverse break-down voltage.

$$R_{on} \propto \frac{V_{BR}^{2.5}}{\text{Area}} \quad (2.1)$$

Many power MOSFETs can typically be turned on and off as fast as 30ns which is ideal for 20kHz ac/ac PDM converters. The on-resistance, however, limits the power density and increases losses. These are considered drawbacks of the device in this

application. In general, one has to sacrifice the breakdown voltage rating for drain current rating or vice versa. For example, a 1000V MOSFET can carry only 1A but a 50V MOSFET can carry 75A or a 200V MOSFET can carry 30A. With these rating, MOSFETs have relatively low power density compared to power BJTs.

Power Bipolar-Junction-Transistors (BJTs)

The Power BJT (Fig.2.2) is a minority carrier device in which current essentially conducts by diffusion. While on, a power BJT requires continuous base current $i_B \geq i_C/h_{FE}$, where i_C is the collector current and h_{FE} (or β) is called the dc current gain which in power BJTs has typical values of 5 to 20. Although h_{FE} decreases quite rapidly at high collector current, it stays fairly constant below the rated current of a power BJT, $I_{C(max)}$. Unlike a MOSFET, when fully on or saturated, a power BJT acts like a voltage source with a value of $V_{CE(sat)}$ opposite to the polarity of the collector current, i_C .

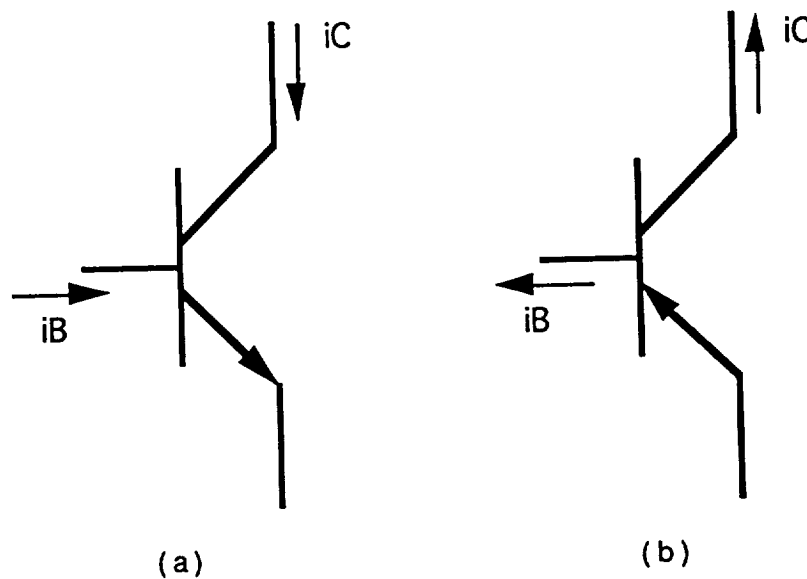


Fig. 2.2 Circuit symbol for (a) NPN, (b) PNP BJT

A power BJT supports forward voltage blocking capability. The blocking capability is due to the lightly doped n-region in the collector. It is relatively resistive until it is conductivity modulated. The large n-region required to block high voltages, however, require injecting more excess carriers to turn on. Thus during turn off these addition carrier must be removed. The cost for higher blocking voltage is higher on-voltage drop, slower switching, longer voltage rise-time and current fall time. In addition, there is a significant change in turn-on and turn-off times at different current levels. Therefore, a power BJT should not be used as a switching device in a power converter that requires critical timing, such as an ac/ac PDM converter.

One method used to avoid hard saturation and thereby speed the turn-off is the Bakers Clamp[7]. An example of such a circuit is shown in Fig. 2.3. This circuit has the disadvantage of increasing forward drop and thus increasing power losses.

Another disadvantage of power BJTs is that the dc gain at higher current levels decreases, thus resulting in higher power requirements from the drive circuits.

Thyristors

Although a thyristor is not a fully controlled switching device, its ruggedness, current density and bi-directional voltage blocking capability makes it still very common in many high power circuits. Fig. 2.4 shows the symbol and model of a thyristor; it consists of one PNP and one NPN transistor. To turn-on, a thyristor needs to be forward biased and have a gate trigger current pulse, i_g . This enables the two back-to-back power BJTs to be in the self-regenerative mode. When in the self-regenerative process, the base of each transistors is driven by the collector of the other. Either reverse biasing or zero current can turn the device off. When turning a thyristor off, a delay time t_q (about 5-10 μ s for fast thyristors) is needed before the thyristor regains forward voltage blocking capability. When off, the combination of NPN

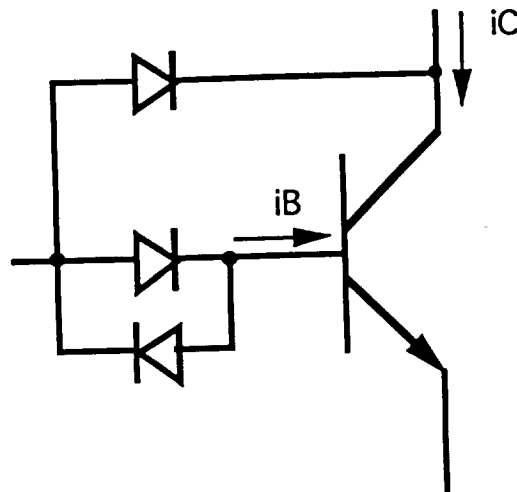


Fig. 2.3 Using a Baker's Clamp Circuit to avoid hard saturation

and PNP can block high forward voltage and their long base can block reverse voltage. In most cases, turn-off of thyristors requires commutation circuits which reverse biases the devices for at least t_q seconds so that the devices leave self-regenerative mode. Usually a commutation circuit dissipates some power, proportional to the switching frequency. This makes thyristors not practical in high frequency switching circuits.

Similar to thyristors, GTOs (Gate Turn-Off thyristors) have high forward voltage blocking capability and current density. The reverse blocking voltage is, however, small. GTOs are used for high power applications in which devices with

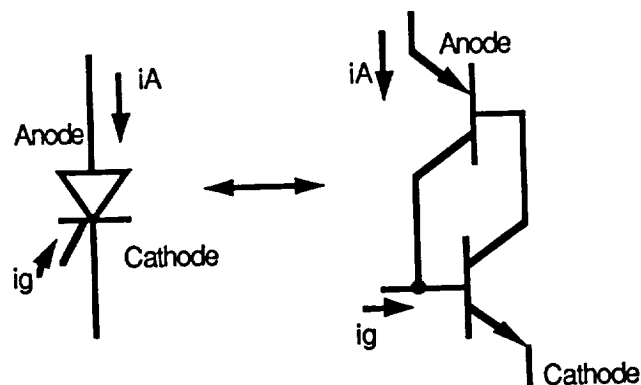


Fig. 2.4 Thyristor symbol and model.

blocking voltage capability of over 1000V are required. Turn-on is like that of thyristors, but turn-off is achieved by a reverse current pulse out of the gate. The actual turn-off mechanism is very complicated and will not be discussed here. Turn-off current gain β_{off} , i_A/i_g , ranges from about 0.2 to 0.5. Therefore, to turn off a high anode current, the drive circuit needs to supply high current pulses. The switching speed of GTOs is limited to about 10kHz.

Insulated-Gate Transistors (IGTs)

At this point, it can be concluded that majority carrier devices have the advantages of high switching speed and are easy to drive, whereas minority carrier devices have the advantages of high blocking capability and high current density. By combining these devices, the advantages of both might be obtained. For example, the (Insulated-Gate-Transistor) is a hybrid device that combines the advantages of both MOS and Bipolar devices. Figure 2.5 shows the structure and model of an IGT.

Like other power devices, the IGT has a lightly doped drift region which is required to block the forward voltage when the device is off. When there is a positive voltage applied across the gate to emitter terminals, a channel is created in the p-base which lets the minority carrier injected into the N-drift region. Although the IGT is modeled as a MOSFET and a PNP power BJT in a Darlington structure, the turn-on and turn-off mechanism are not the same as in power BJT. When off, the P+ substrate, n-drift region and the P base in IGT acts like two back-to-back diodes. Since the n-drift region is lightly doped and relatively longer than that in ordinary diodes, these two diodes can block bidirectional voltage.

The blocking voltage of the two diodes can be asymmetrical in higher current rating IGTs. This is because the n-drift region is shorter in order to reduce the on-resistance. The breakdown voltage is then reduced. However, the addition of n+ buffer

(not shown) prevents punch-through breakdown when the device is blocking forward voltage but it does not protect the reverse breakdown.

To turn the device on, a positive gate-to-emitter voltage is applied and a channel is then induced in the p-base. Majority carriers are injected into the n-drift region through the channel whose resistance will be decreased as more and more majority carriers collect in this region. This is because the n region is under high level injection or conductivity modulation, which behaves like a forward biased PIN diode [6]. The main difference between a Darlington structure and an IGT is that the MOSFET, rather than the collector of the pnp transistor, contributes to a major part of the total device current. The voltage fall time during turn-on depends on how fast the n-region is conductivity modulated.

Turn-off of an IGT is achieved by applying negative gate to emitter voltage. The collector-to-emitter voltage rise time is as short as in a MOSFET because only the channel carriers are needed to be removed. However, the current fall time is known to have tail due to the excess carriers in the n-drift region. With the IGT structure, there is no way of applying reverse voltage to the base emitter junction to help remove excess carriers in the n drift region. The only way is by recombination which will take a longer time.

Although IGTs has the best features of MOSFET and BJTs, that is voltage-control and high current density, the on state voltage drop due to the MOSFET at high current and the current tail at turn off still constitutes power losses especially at high switching frequencies. A better device should then have the best features of IGT but low and constant on state voltage drop. The MOS-Controlled Thyristor(MCT), a newly emerging double mechanism hybrid device, may meet the requirement for a better device.

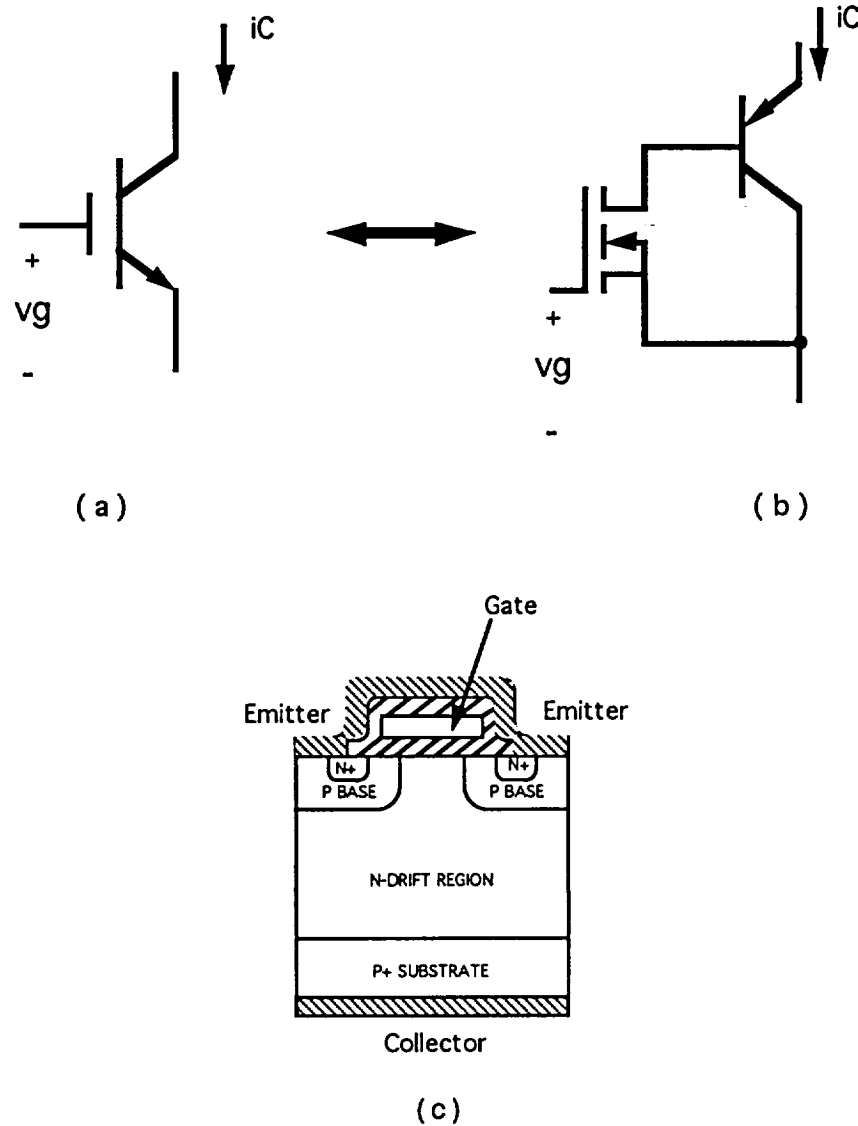


Fig. 2.5 (a)The circuit symbol, (b) simplified Model and (c) structure of IGTs

2.2 The Mos-Controlled-Thyristor (MCT)

Current research in new device technologies has led to devices that combines the power handling capability of thyristors and the fast switching characteristics of power MOSFETs. In particular the MCT, a newly emerging device that combines the high current density and ruggedness of a thyristor with the ease of control of a MOS gate,

continues to be the promising power switch for the next decade. Researchers continue to develop the static and dynamic characteristics of the MCT.

The MOS-Controlled-Thyristor (MCT) is double mechanism device. It can be modelled as two MOSFETs and a thyristor as shown in Fig. 2.6. The on-MOS and off-MOS in the model are p-channel and n-channel respectively. As described above, turn-on of a thyristor requires only a current pulse which triggers a self-regenerative process. However, the MCT is a level turn-on and turn-off devices which does not reflect the characteristic of a thyristor and will be explained later.

To understand the operation of an MCT, one should start from the switching mechanism of the MOSFETs and BJTs. As a negative voltage, V_{AK} , applied to the gate relative to the anode, the PMOS is turned on, thereby, the base of the npn transistor will be shorted to the anode and then supplied with plenty of base current. Since the NMOS is off, the base of the pnp transistor becomes the only path that supplies current to the collector of the npn transistor so that the pnp transistor is also turned on. Thus a self-regenerative process by these transistors keeps the MCT on. This mechanism is similar to that of a regular thyristor. Due to its thyristor structure the MCT has a lot higher current density than the similar device IGT.

Note that even if an MCT has been latched on, the gate voltage, V_{GA} , has to, remain negative. This is because the off-MOS should be completely off and not interrupt the self-regenerative process by sharing current with the base of the pnp transistor.

Unlike a thyristor, the trigger current is not supplied externally but through the p-channel from the anode. There must be some threshold voltage across the anode to cathode, V_{AK} , and should be high enough to start a regenerative process. This threshold voltage has been reported to be as high as 90V for some MCTs [7], which makes the device not suitable for zero-voltage-switching circuits like PDM converters. This problem will be discussed and solved in a later chapter.

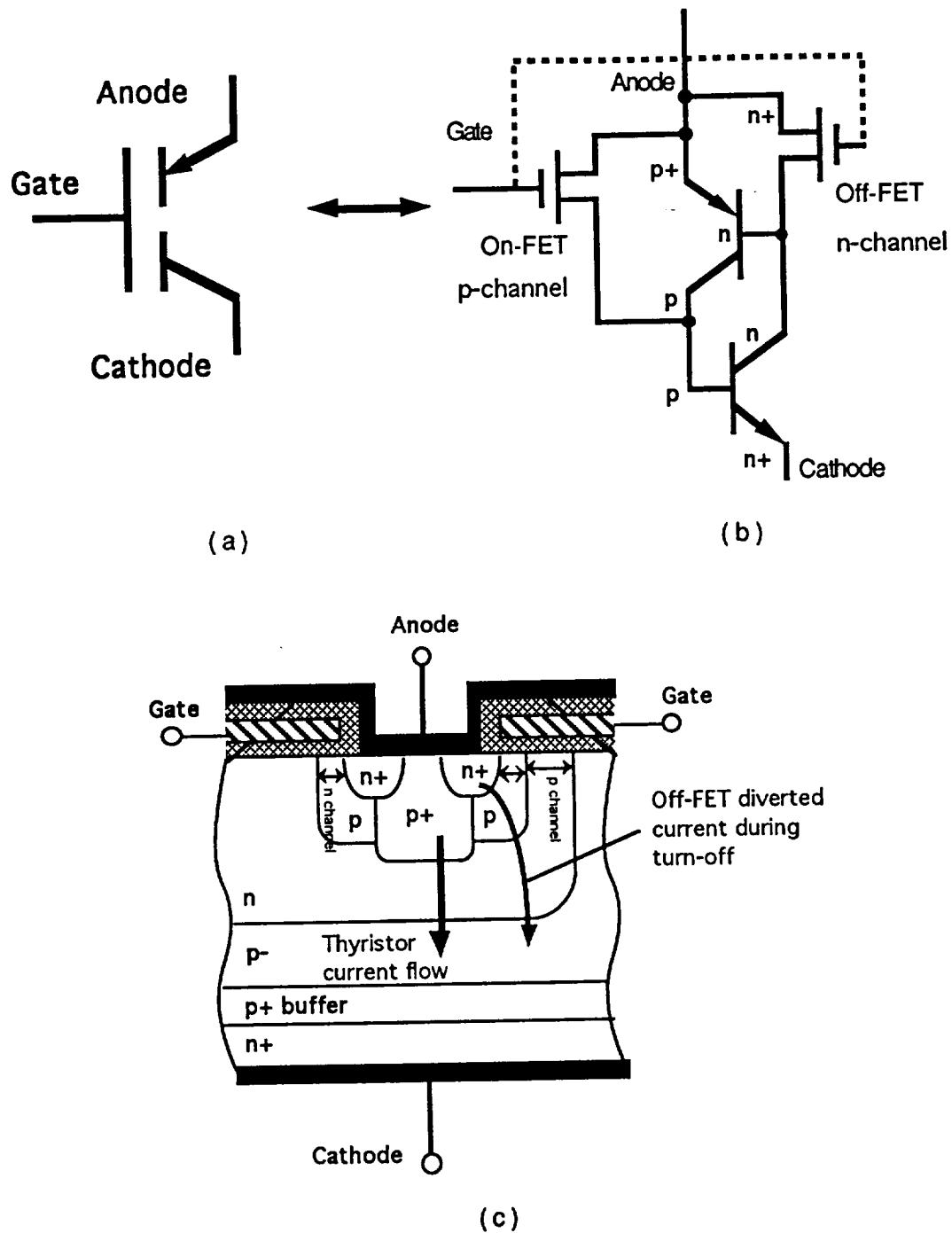


Fig. 2.6 (a) The circuit symbol, (b) the model and (c) the layout of an MCT.

Turn-off of MCT requires a positive gate voltage, V_{GA} , to turn the NMOS on and the PMOS off simultaneously. As the NMOS is turned on, the emitter is then shorted to the base by the low resistant n-channel. V_{EB} of the pnp transistor becomes less than the

necessary on-voltage (forward voltage across a pn junction), thus there is no base current to keep the transistor on. As a result, the pnp transistor no longer supplies current to the base of the npn transistor, and the self-regenerative process is then stopped. After all the excess minority carriers in the bases of both transistors have recombined, the MCT is turned off. When off, the gate voltage, V_{GA} , has to remain positive lest the PMOS might re-trigger the base current of the npn transistor.

Because of the channel resistance, at some high current level, the NMOS may not be able to force an active short circuit across the emitter and the base of the pnp transistor due to its channel voltage drop. The MCTs, therefore, cannot be turned off by the gate at too high of current. It also needs higher gate voltage to turn off higher current.

With its thyristor characteristics, the MCT has potential symmetric bi-directional voltage blocking capability. However, the reverse voltage blocking is still under research.

The features of an MCT are summarized as the following: gate-voltage turn on and off, low power gate drive circuit like a MOSFET, high current density, ruggedness, low and consistent forward voltage drop, asymmetric (but potentially symmetric) voltage blocking capability. Even though the switching speed is less than 50kHz, with its best features of both the MOSFET and thyristor, the MCT still closest to the ideal switch among the existing power devices.

2.3 The MCT in Bi-directional Switch Configurations

Bi-directional switches are used in power electronic circuits that deliver reactive power and have ac voltage source input, for example, ac/ac converters. Except for the triac (Fig. 2.7), most power devices do not have bidirectional current conduction and voltage blocking capabilities. However a triac is not a fully controlled device, that is, it cannot be turn-off by applying a gate signal. Therefore, construction of

bidirectional switches often need additional power diodes to block reverse voltage. Different configurations of these switches will be considered in this section.

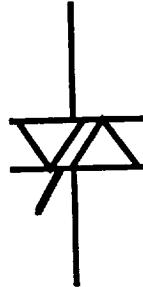


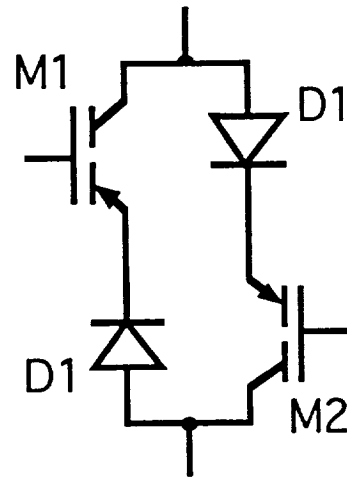
Fig 2.7 Circuit symbol of a triac

In Fig. 2.8, there shows four major kinds of bidirectional switch configurations. Although in the figures it shows only MCTs, the switching devices in these configurations can be any fully-controlled devices. Each configuration has its advantages over the other and will be briefly discussed.

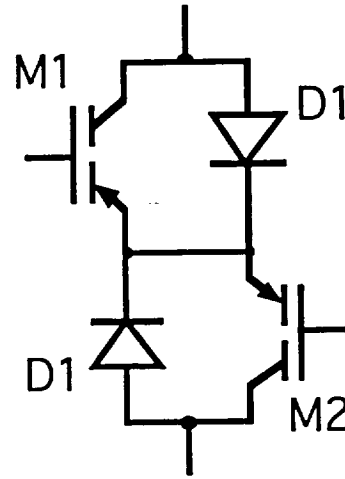
All the diodes in Fig 2.8(a), (b) and (c) are responsible for blocking reverse voltages. If a device has bi-directional voltage blocking capability, it can be used in the configuration of Fig 2.8(d) and no series diode is needed. The main advantage of the circuit in Fig 2.8(d) is that it has the minimum forward voltage drop out of all other configurations.

Many power devices have built-in anti-parallel diodes as shown in Fig.2.9. In some cases, if these diodes cannot provide satisfactory performances, they should be bypassed by connecting as in Fig 2.8(a) and (c). Conversely, if these built-in diodes can be used in configuration Fig. 2.8(b), the two external diodes are not necessary thus the circuits cost less and have smaller size. The difference between Fig. 2.8(a) and Fig. 2.8(b) is a common node in the middle.

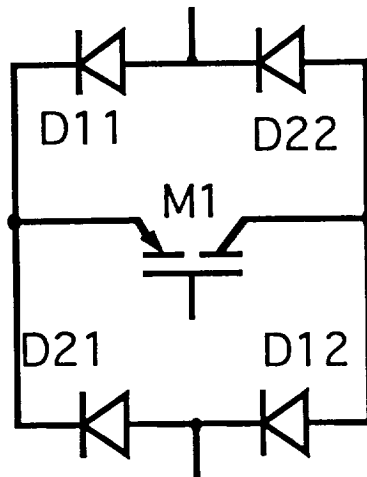
To turn on the switches in Fig. 2.7(b) and (c), only one gate signal is needed. The main features of each configuration are summarized in Table 2.1.



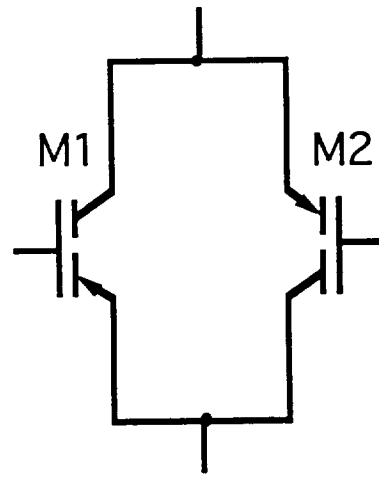
(a)



(b)



(c)



(d)

Fig 2.8 Bidirectional switch configurations

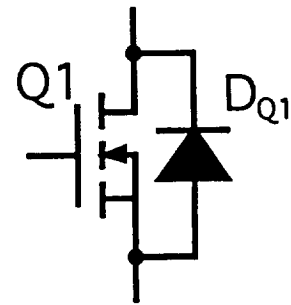
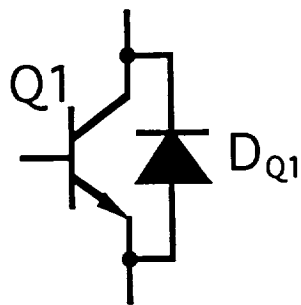


Fig. 2.9 Examples of power devices with built-in anti-parallel diodes.

	Number of isolation gate drive circuits needed	Forward Voltage Drop	Requirement of devices able to block Bidirectional voltage	Number of switching devices required in a 3- phase ac/ac PDM circuit
Fig 2.7(a)	2	$V_M + V_D$	No	2
Fig 2.7(b)	1	$V_M + V_D$	No	2
Fig 2.7(c)	1	$V_M + 2V_D$	No	1
Fig 2.7(d)	2	V_M	Yes	2

Table 2.1 Summary of the Bidirectional switch configurations

High forward voltage drop contributes to significant power losses which are always the main concern in many converters. Therefore configuration (c) should not be used in high power circuits due to its high forward voltage drop (one device plus two diodes). If bidirectional voltage blocking devices are available, configuration (d) should always be considered first because it has the lowest on-voltage.

If MCTs are used in a three phase ac/ac PDM circuit as in Fig. 2.10, the switch configurations in Fig. 2.8(d) can be used. Twelve MCTs are used. As mentioned before, the best feature of this configuration is the low on-voltage drop which the on-voltage of an MCT and is about 1.2V at 60A [Appendix A].

The number of isolated gate drive circuits needed to control one single switch does not reflect the number of those in a three phase converter. For example, although the converter of Fig. 2.11(a) needs twelve gate drive circuits, only five isolated power supplies are needed because there are five nodes sharing common anodes (one in the top rail, one in bottom rail and three in the middle).

This configuration requires the MCTs to have bi-directional voltage blocking capability, but the currently available MCTs do not have the reverse blocking capability. Therefore the next best bidirectional switch configuration was used. External diodes were needed to block the reverse voltage. Fig. 2.11 shows two possible ac/ac PDM converter circuits using the switch configuration in Fig. 2.8(b). Although extra diodes are added and will contribute some voltage drop, both Fig. 2.11(a) and (b) have an on-voltage only about 2V at 60A which is still very low compared to many other existing power devices, e.g a thyristor.

The converter shown in Fig. 2.11(a) obviously requires six isolated power supplies and six gate drive circuits to control six bi-directional switches. As the

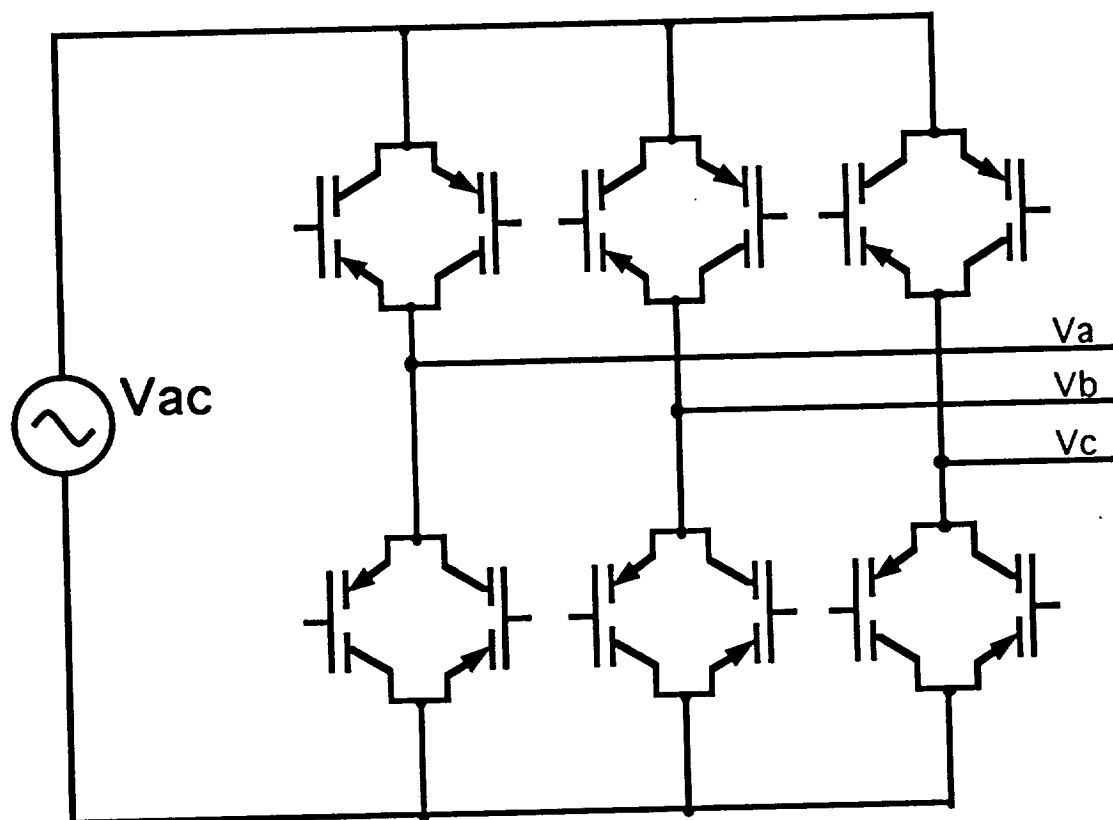
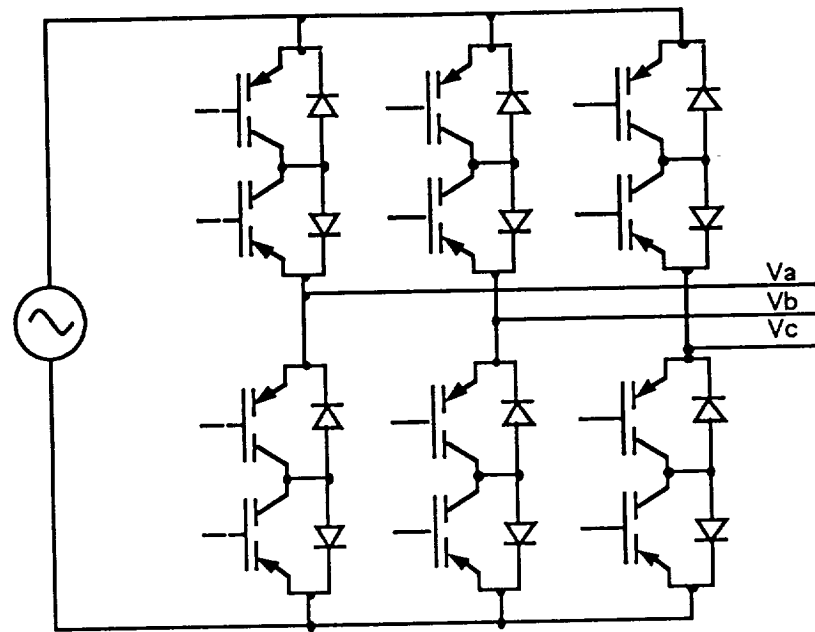
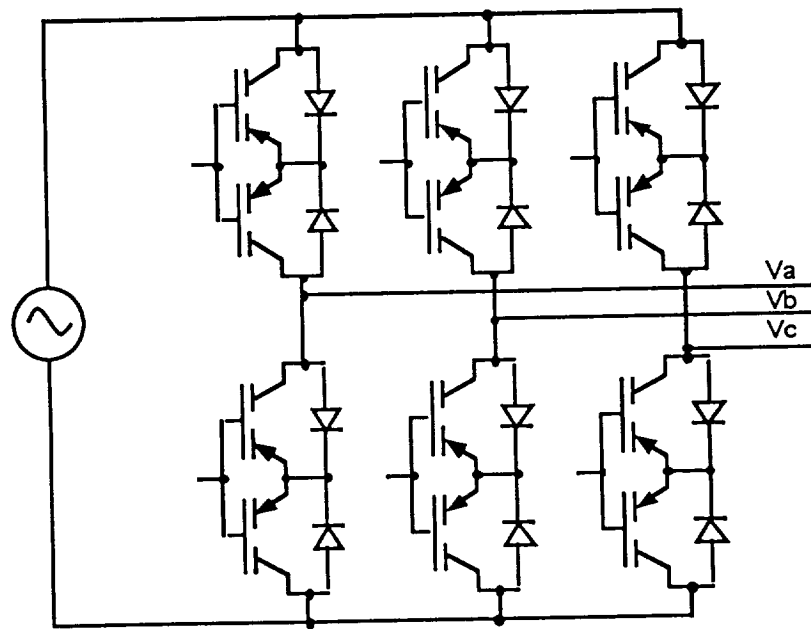


Fig. 2.10 Three phase ac/ac PDM inverter using twelve MCTs. It requires the MCTs to be able to block voltage in both forward and reverse direction.

converter shown in Fig. 2.11(b) has five common anodes, it only needs five isolated power supplies. Although it saves one power supply, it needs twelve gate drive circuits because the two gates in each bidirectional switch cannot be shorted together. Roughly speaking, six more gate drive circuits is about the same cost of one simple power supply. In practical cases, from the size and weight point of view, saving one power supply is more preferable. However in this research, enough power supplies are available, size and weight are not the issues. Using six control signal is actually better for researches because it makes it easier for trouble-shooting. The circuit shown in Fig. 2.11(a) are used in this report.



(a)



(b)

Fig. 2.11 Three phase ac/ac PDM inverter using twelve MCTs and twenty four diodes. They do not require the MCTs to have bidirectional voltage blocking capability. (a) Six isolated power supplies are needed but only six drive circuits. (b) Needs five isolated power supplies but twelve gate drive circuits.

CHAPTER III

TESTING OF MOS-CONTROLLED THYRISTORS (MCTS)

Although commercial MCTs were not yet available during the time of this research, samples of developmental TO-218 packaged MCTs were obtained from Harris Semiconductor™. The samples were tested and studied in two prototype circuits; a dc chopper with current source load (Fig. 3.1) and a single phase 20kHz resonant ac link PDM converter with 4kHz current source load (Fig. 3.2). Both the prototype circuits were switched at 20kHz, which is the frequency used in in space station applications. The primary purposes of testing the devices are to characterize the transient behaviors under hard and soft zero-voltage switching conditions. The test results were used to predict and analyze the advantages and disadvantages of using MCTs in a three phase ac/ac pulse-density-modulation (PDM) converter. The samples used in this research has $I_{RMS} = 60A$ and $V_{DRM} = 600V$ which gives a very high power density for a TO-218 packaged device. Additional information about the sample MCT is shown in Appendix 1.

3.1 Testing of MCT under hard switching

3.1.1 Procedure

The prototype dc/dc down converter using an MCT is shown in Fig. 3.1. The diode used in this circuit is an ultra-fast recovery one and can match the switching speed of an MCT. The output voltage is controlled by the duty ratio (D) of the MCT. Such a circuit is found in applications like dc motor drives, automotive power supplies, battery chargers etc. In this test circuit, the time constant $L/R = 800\mu s$ is much larger than

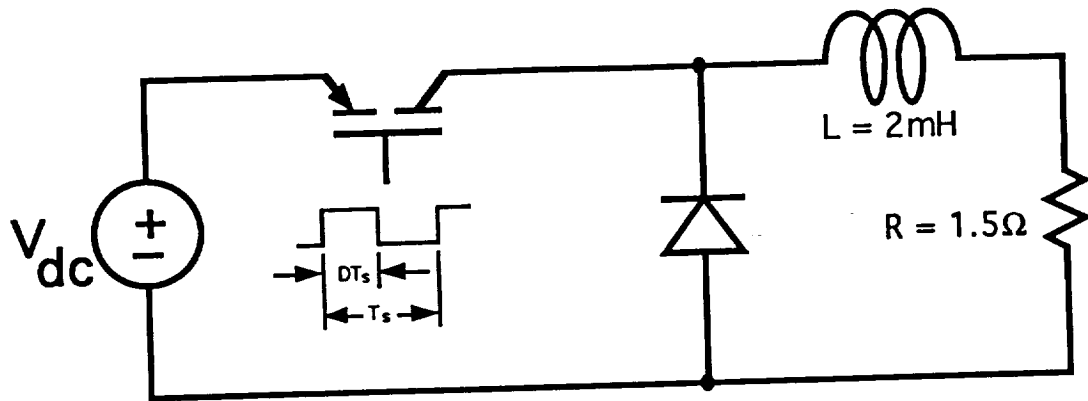


FIG. 3.1 A dc/dc down converter.

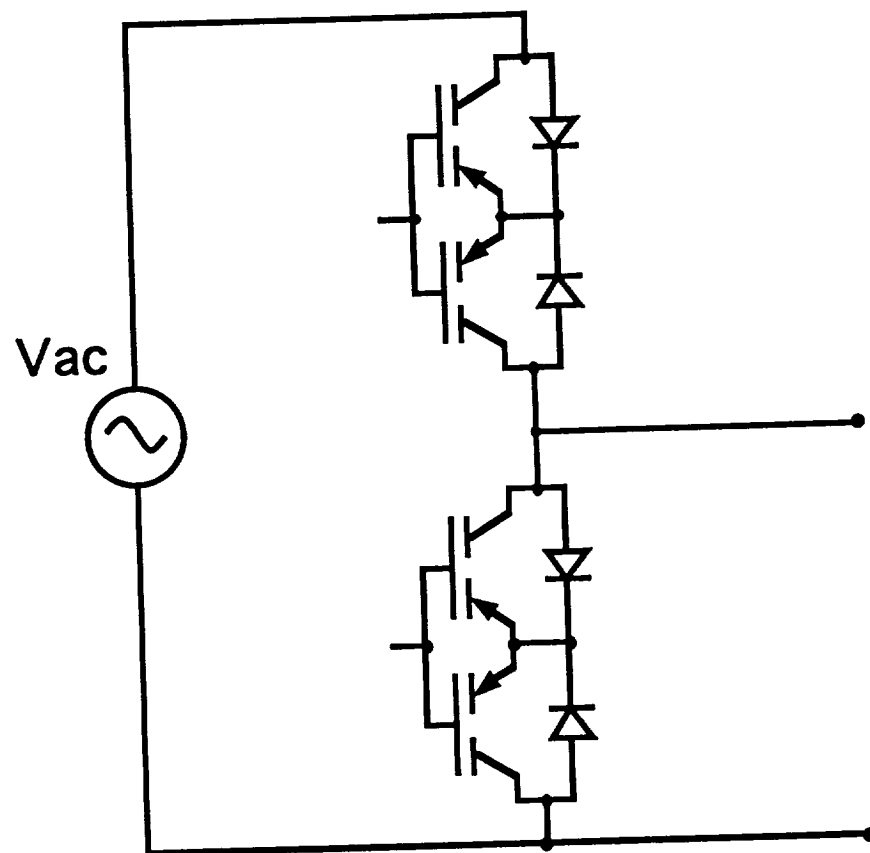


FIG. 3.2 A single phase PDM converter.

the switching period, $T_s = 50\mu s$, therefore the load current is continuous, has low ripple and can be modeled as a current source. Since the diode is reverse biased as soon as the MCT is turned on, it forces the device to pick up the load current immediately. At

turn-off, the MCT has to block a forward voltage, V_{dc} , instantaneously. Although the ultimate goal was not to use any hard switching topology in the converter, the objective of this circuit is to find the gate drive requirement, capability of switching at 20kHz and understand more about the characteristics of the device.

From the data sheet supplied by Harris Semiconductor™, a typical turn-off loss at 300V and 120A is about 30mJ. The maximum power dissipation of the device at the room temperature, 25°C, is 208W and will derate at 1.67W/°C above the room temperature. Clearly, with this much turn-off loss the MCT is, however, not able to switch at 20kHz at the same power level as the Harris Semiconductor™ test circuit unless a high wattage turn-off snubber is used. Therefore, in this hard switching experiment, the intended voltage and current levels were not close to the maximum rating of the device.

Because the device was assumed to be MOS-gated, the gate drive circuit was similar to that of a MOSFET. A simple signal-level BJT push-pull gate drive (Fig. 3.3)

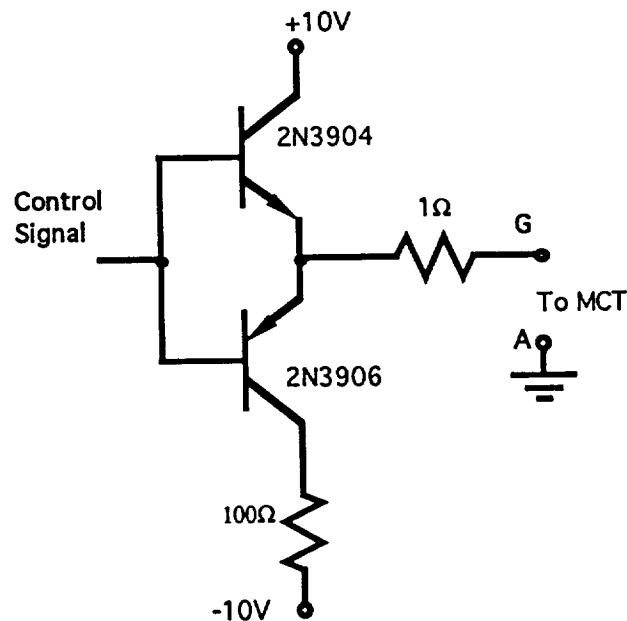


Fig. 3.3 A simple push-pull gate drive circuit.

was, therefore, used in this experiment. The circuit rise time of the gate signal was $0.2\mu\text{s}$ without the MCT and $3\mu\text{s}$ with an MCT connected.

3.1.2 Results and Comments

In the beginning, a number of failures of MCTs were encountered while the circuit was operating below 10A and 50V . Also, there was a thermal runaway problem. Although most of the time, the MCTs could survive thermal runaway, the damage was first assumed to be related to excess thermal dissipation at 20kHz .

Two possible problems might have caused the excess thermal dissipation: (1) the device not being fully turned on or off, (2) the requirement of a turn-off snubber. However, it was obvious that the device fully on when it was supposed to be on.

To reduce the device failure rate both procedures and circuits were modified. Additional care was also taken when handling the MCTs. A cooling fan was installed to increase the rate of air-flow. The turn-off gate voltage, V_{GA} , was increased from 10V to 15V so that the device would turn off harder. A turn-off snubber circuit was also added in parallel with the free-wheeling diode, as shown in Fig. 3.4. The capacitor limited the rate of change of voltage across the MCT so that $I_A \cdot V_{AK}$ became smaller at turn-off. The mechanism of this snubber circuit will be discussed in Chapter Four.

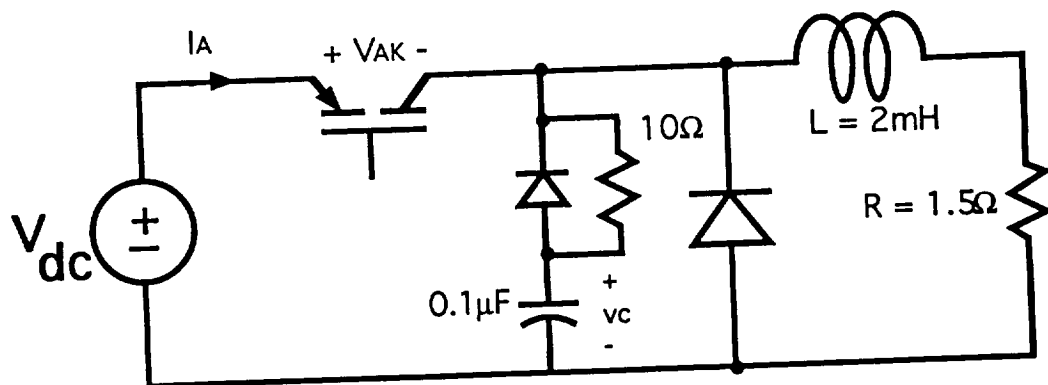


Fig. 3.4 Turn-off snubber connected in parallel with the diode to limit the dV_{AK}/dt when the MCT is turned off.

It had also been found that in order to switch the device safely the gate signal should have a fast rise time of about 200ns [8]. This is required to have all the cells in the MCT act in unison and thereby avoid "hot spots" [9]. The gate-to-anode has a static capacitance of about 0.01 μ F. In order for the gate voltage changes from -20V to +20V in 200ns or less, the drive circuit should be able to supply 2A and have a large bandwidth.

The drive circuit of Fig. 3.3 is, however, unable to provide that high of a rise time. An improved drive circuit (see Fig. 3.7) was designed to meet the requirements. In addition to the conventional push-pull transistor pair, the output stage has two complementary power BJTs, ECG377 and ECG378, with $f_T = 50\text{MHz}$, so that the gate of the MCT was driven by both the collectors of the power BJTs and the emitters of the signal transistors. In the first amplifier stage, the transistor was switched between cutoff and saturation. The collector and emitter resistors are used as a voltage divider so that the output of this stage is either at 15V(cutoff) or -10V(saturation)

After the changes were made, some improvement was observed. The power could be pushed to a higher level before thermal run-away happened and no more failures were encountered in the hard switching test circuit. The MCT was then switching at 20A and 70V (which is the maximum output voltage of our dc supply at this high of load current) at 20kHz. Figures 3.5 and 3.6 shows the current and voltage waveforms.

The current waveform in Fig. 3.5, without a turn-off snubber, has a longer tail at turn-off compared to that in Fig. 3.6. Without a turn-off snubber the thermal dissipation caused the temperature to increase. As the device temperature increased, it took a longer time for the excess minority carriers in the base to recombine thus causing a longer current tail and more thermal dissipation at turn-off. This further increased the temperature which and, in turn, increased the current tail.

To summarize the hard switching experiment, the MCT dissipated power at turn-off that could cause thermal run-away. A turn-off snubber was needed at high switching frequencies. The gate drive should be able to provide a rise time of 200ns so that the MCT could be switched safely.

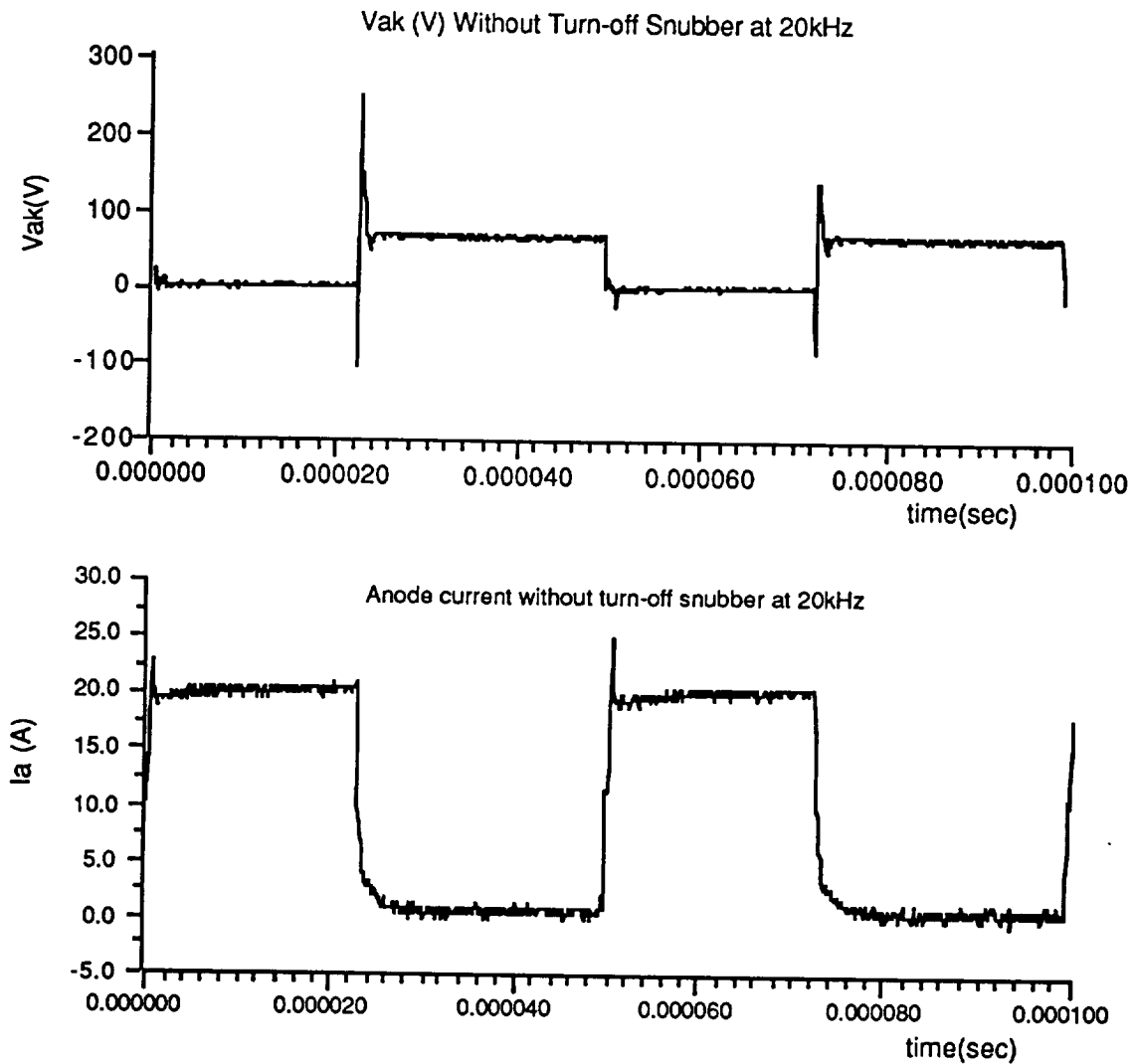


Fig. 3.5 Hard switching waveforms without snubber.

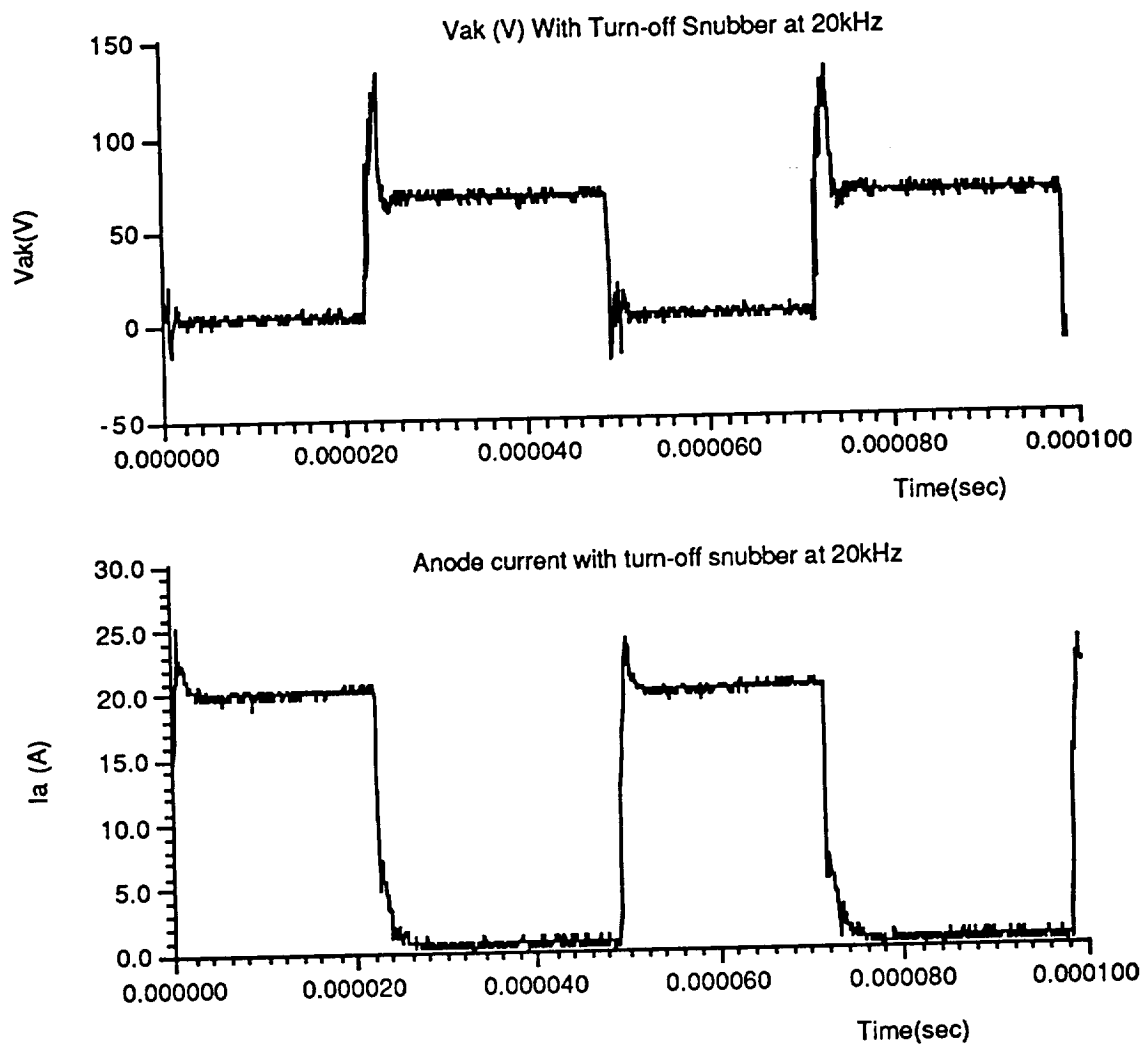


Fig. 3.6 Hard-switching waveforms with snubber.

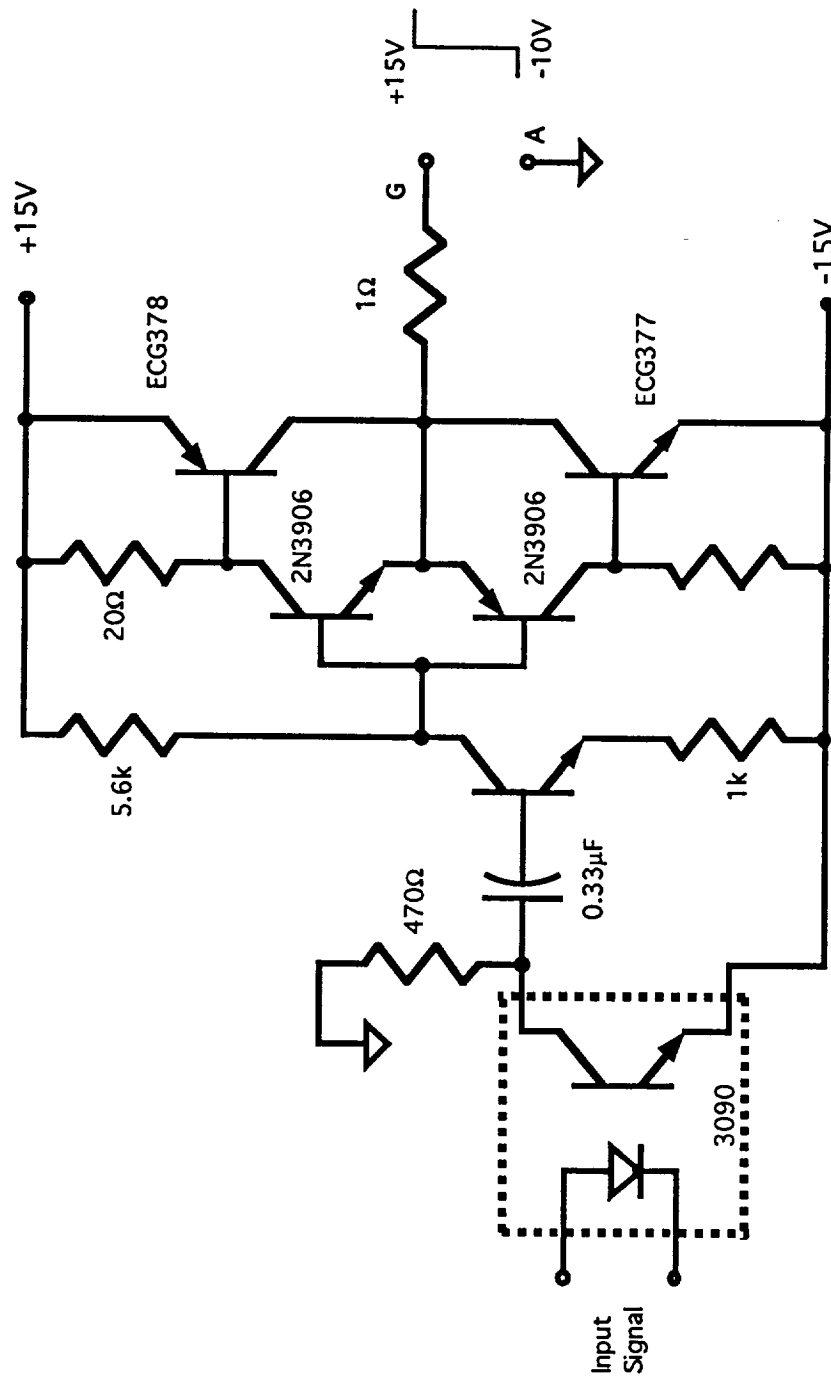


Fig. 3.7 An improved gate drive circuit that can provide 200ns rise time

3.2 Testing of MCT under soft switching

As mentioned above, theoretically MCTs cannot be turned on at zero-voltage. Also, it had been reported that the MCT requires as high as 90V threshold cathode-to-anode voltage to turn-on [7]. In spite of the problems of switching an MCT at zero-voltage, the main objective of this experiment was to test the device under zero crossing switching, however, with a different test circuit than in [7]. With the new circuit it was anticipated better results might be obtained.

A Mapham Inverter [10] was used to supply the 20kHz voltage for the single phase PDM circuit that shown in Fig. 3.2. A series RLC load (instead of an RL load mentioned in Chapter One) is connected to the single phase PDM converter as shown in Fig. 3.8. The resonant frequency of the load was tuned to 4kHz with a very narrow bandwidth which gave 4kHz sinusoidal current source load (I_{out}). Zero-voltage with non-zero-current switching behavior was observed. Figure 3.9 shows the idealized waveforms and control signals to the switches S1 and S2. Note that each switch consists of two MCTs and two diodes. This bi-directional configuration was discussed in Chapter Two.

3.2.1 The Block Diagram

A schematic of the single phase PDM converter is shown in Fig.3.10. The output of the Mapham inverter is the 20kHz high frequency ac link, V_{ac} , as shown in Fig. 3.9. S1 and S2 are switched at zero crossings of the high frequency ac link.

3.2.2 The Zero Crossing Detector With Compensation

Note that the duration of every half-cycle of V_{ac} is only 25 μ sec. Without compensating for the delays in the control logic, the gate drive circuits and the MCTs, using a simple comparator type zero-crossing detector may cause an error significant enough that zero-voltage-switching cannot be achieved. For example, a delay of

4.17 μ sec (30°) makes the converter switch at half of the peak voltage of V_{ac} instead of near zero voltage.

A more precise zero-crossing detector, as shown in Fig. 3.11, was designed for applications where critical timing is required. The circuit consists of a slope detector and a comparator with hysteresis. It simply shifts the zero-level by some small voltage according to signs of the slope of the input sinewave, therefore instead of detecting zero-crossings, it detects before zero-crossings, thereby, the delays are compensated, an example is shown in Fig. 3.12. The clock, "CLK", from the output of the zero-crossing detector is needed by the sequential logic circuit.

3.2.3 The Control Logic Circuit

As can be seen in Fig. 3.9, the controls signal to S1 has the sequence of "10101 10101 10....." and the control signals for S2 is just the inverse of S1. This sequential signal is obtained using a ring counter. The signal repeats every five clock pulses, i.e. it has five states. A 4-bit counter, 74163, was used because it can store up to 16 states. The timing diagram for the outputs of the counter and the required signal of S1 are shown in Fig. 3.13. To find a Boolean expression for S1 in terms of CLK, Q0, Q1 and Q2, a Karnaugh map, shown in Fig. 3.14, was used. It is found that $S1 = CLK \oplus Q2 + Q0 Q1$. The logic circuit shown in Fig. 3.15 is used to generate S1 and S2 ($= S1'$). Note that Q3 needs not to be used because this circuit does not store more than five states.

One should keep in mind that CLK is the output from the zero-crossing detector discussed in the previous section. Rising and falling edges of the S1 and S2 are, of course, synchronized with CLK and therefore the zero-crossings of the high frequency ac link, V_{ac} .

S1 and S2 are sent to the inputs of two isolated gate drive circuits. The same gate drive circuits as shown in Fig. 3.7 from previous section are also used in this experiment. Unlike in the dc chopper experiment, each drive circuit has to drive two

MCTs (because each bi-directional switch consists of two MCTs and two diodes). The rise time of the gate voltage became longer, but it increased only to about 250ns.

3.2.4 Results And Discussions

The experimental output waveforms of the ac/ac converter agreed with what was expected in the idealized waveforms of Fig. 3.9. The adjustable zero-crossing detector which compensates the delays, the MCTs were switched at zero-voltage. The MCTs being switched at zero-voltage performed satisfactorily.

However the Mapham inverter failed to provide an ideal 20kHz ac source, the voltage and current were limited to a fairly low levels due to saturation and overheating of the resonant inductors in the inverter (appendix III presents some basics about this resonant inverter). The peak voltage and current across the MCTs were only about 70V and 2A respectively. Heat dissipated in the MCTs was unnoticed. The voltages across S1 and S2 are shown in Fig. 3.16. As seen in Fig. 3.17, there is a turn-off delay of about 1.7ms. Therefore, during the delay time S1 and S2 are both on, but this does not constitute a shoot-through problem because the voltage across the switches is essentially zero. During turn-on, it is found that the forward voltage drop across each switch is 1.8V including a diode voltage drop. Fig. 3.19 shows the transient switch currents i_{S1} and i_{S2} . It agrees with the results from the simulation [8] except that it has a longer turn-off time and high frequency ringing. The turn-off time was caused by a longer turn-off delay than was predicted in the simulations. The ringing was caused by the lead inductances reacting with the device capacitances.

As was pointed out earlier the drawbacks of this converter are the requirements of critical timing for switching, and that devices must withstand higher voltage blocking capabilities compared to those of a PWM converter. The timing is critical because each half cycle of V_{ac} has only 25 μ s. If the turn-on and turn-off delays were known and consistent, fixed delay compensations could still be used. At the current level in this

experiment the turn-off delay was found to be $1.7\mu\text{s}$ but as mentioned in the previous experiment, like most devices, the delay times changed at different current levels. In addition, turn-on of one switch and turn-off of the other in one leg have to happen instantaneously. The possible problems that caused by the timing will be discussed in detail in the later chapters.

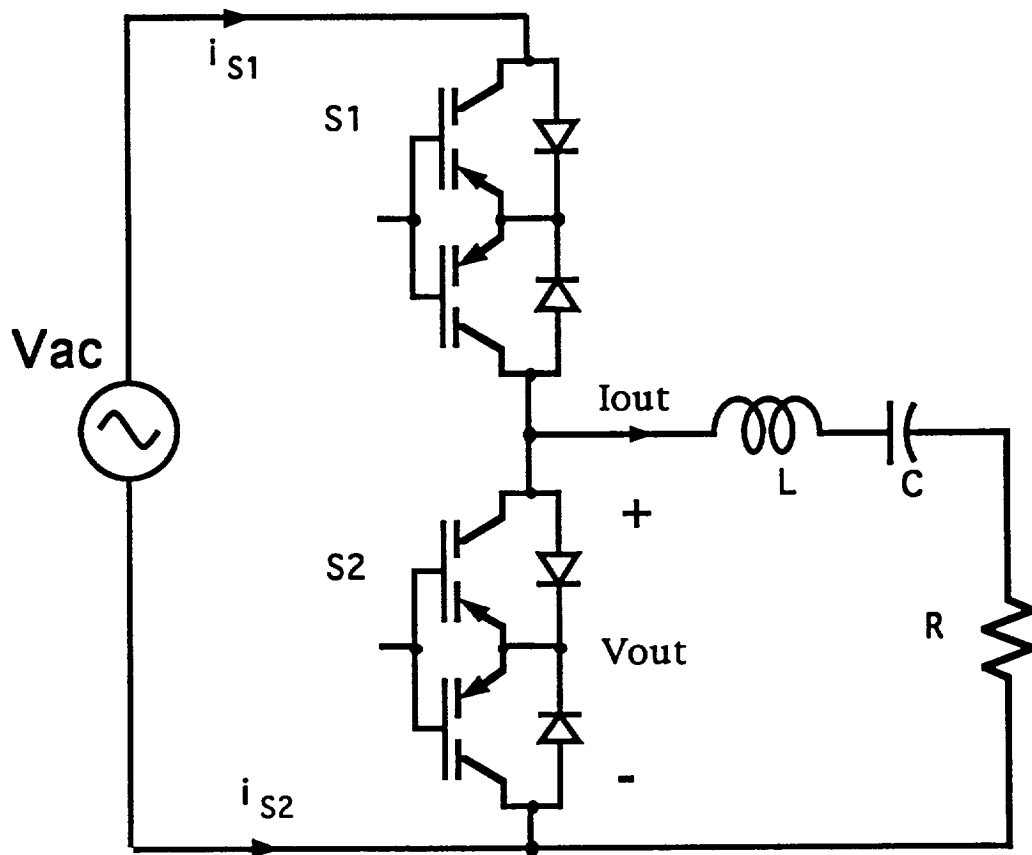


Fig. 3.8 An RLC filter acts like a 4kHz current source load

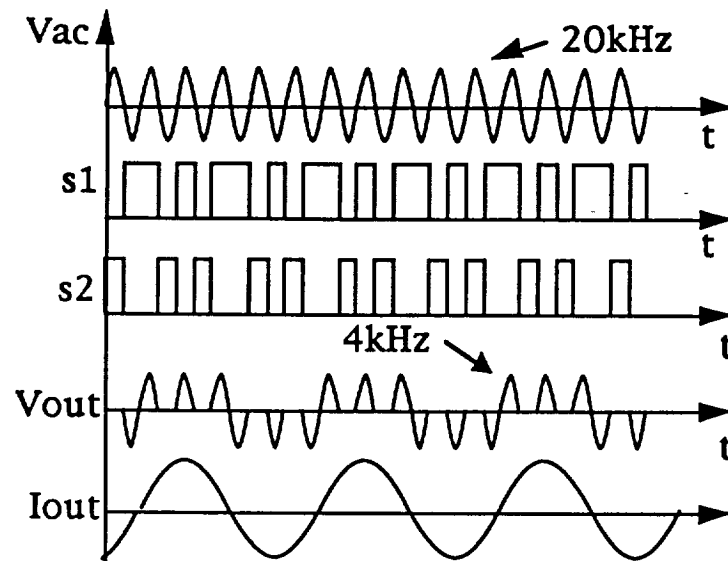


Fig. 3.9 Idealized timing and control of the switches.

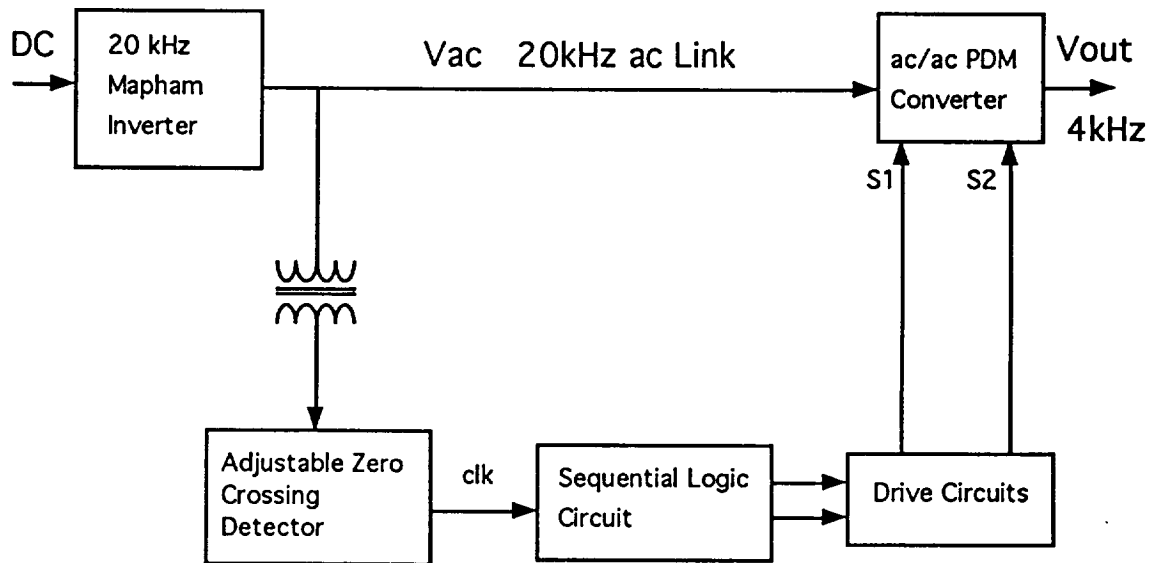


Fig. 3.10 The block Diagram of the power circuit and its controller

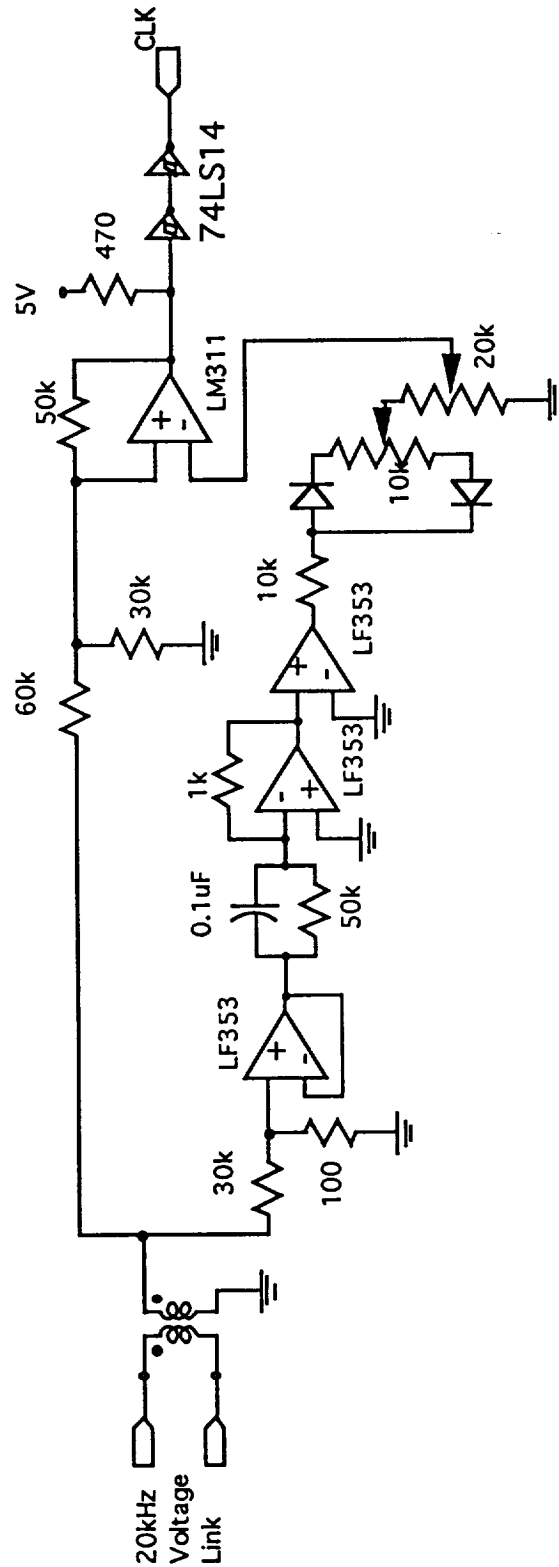


Fig. 3.11 Zero crossing detector that can detect before zero crossing

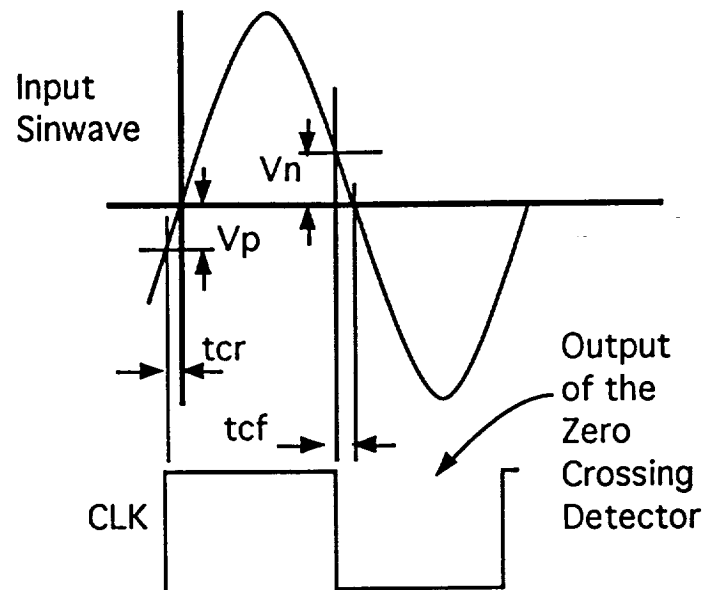


Fig. 3.12 Illustration of the adjustable zero-crossing where V_n and V_p are the adjustable "zero-levels"; t_{cr} and t_{cf} are the positive- and negative-going zero-crossing compensations respectively.

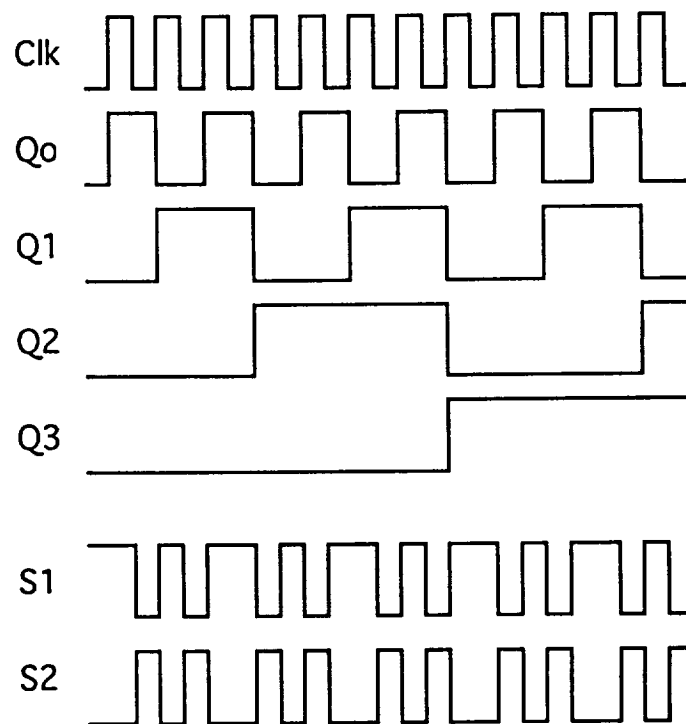


Fig. 3.13 Timing diagram for the outputs of the ring counter and the control signals of S1 and S2

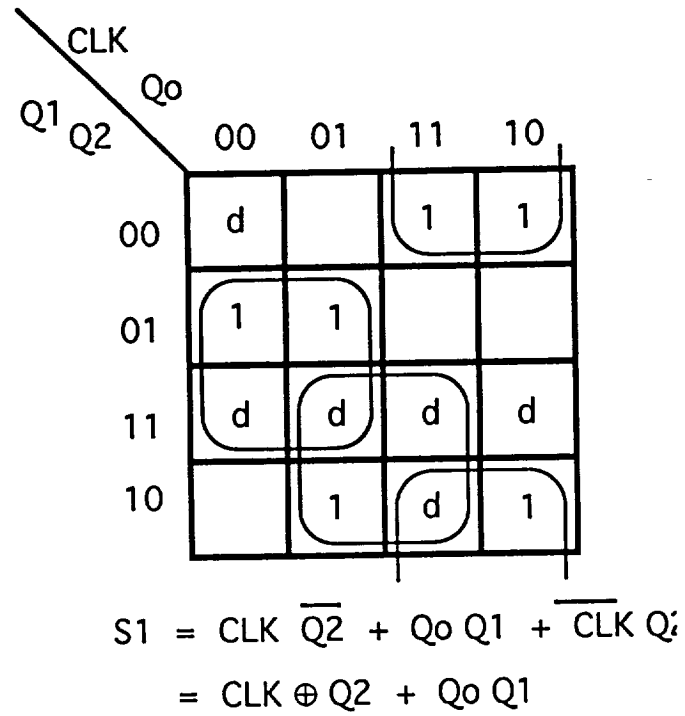


Fig. 3.14 Karnaugh Map for the control signal of S1

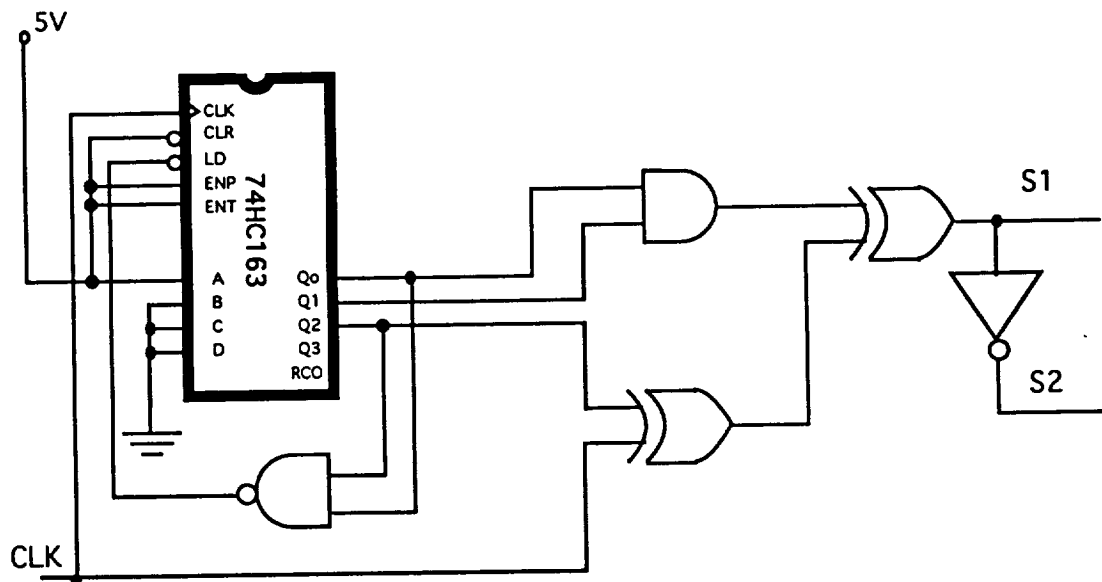


Fig. 3.15 Circuit that generates the control signal for S1 and S2

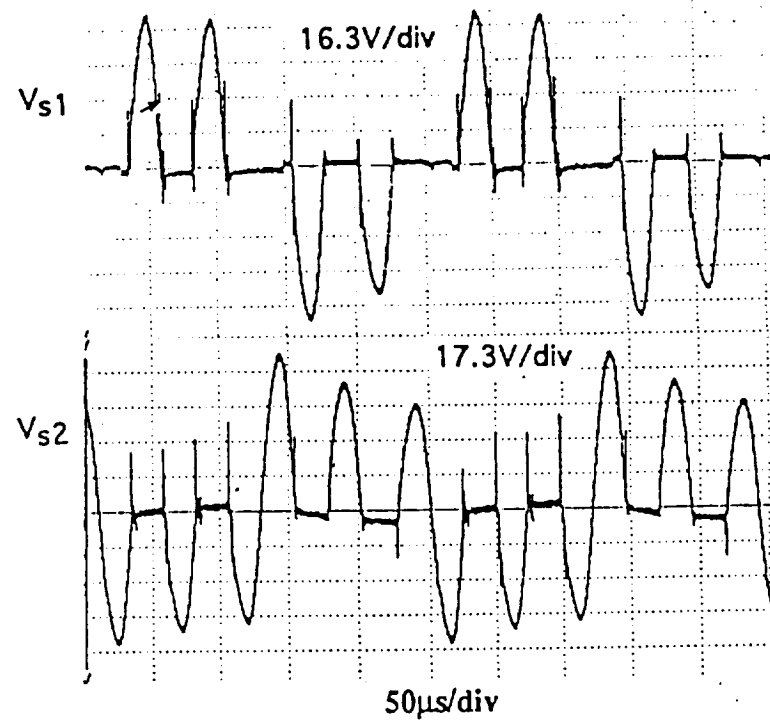


Fig. 3.16 Voltage across the switches S1 and S2

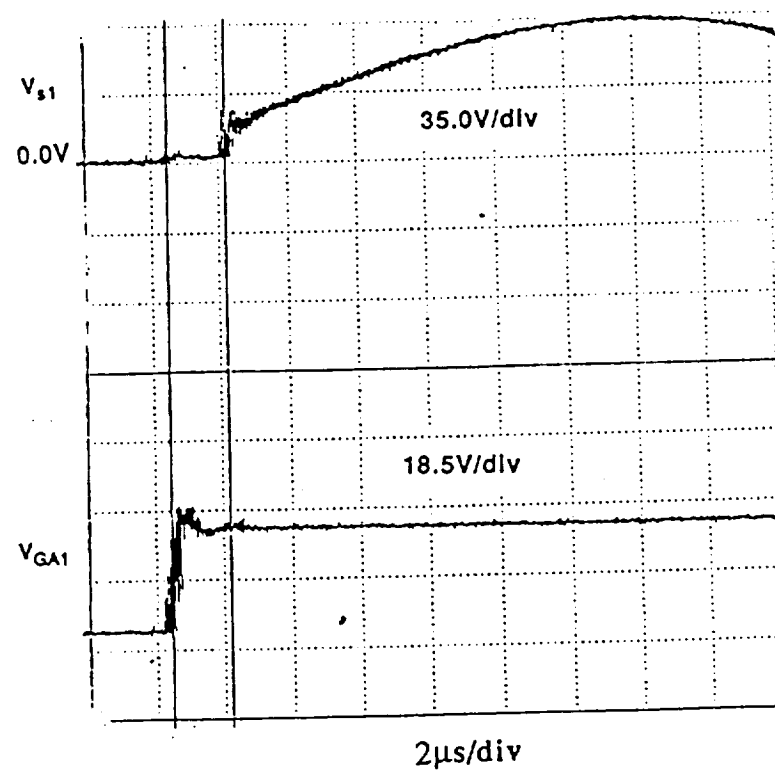


Fig. 3.17 detail of voltage rise during turn-off

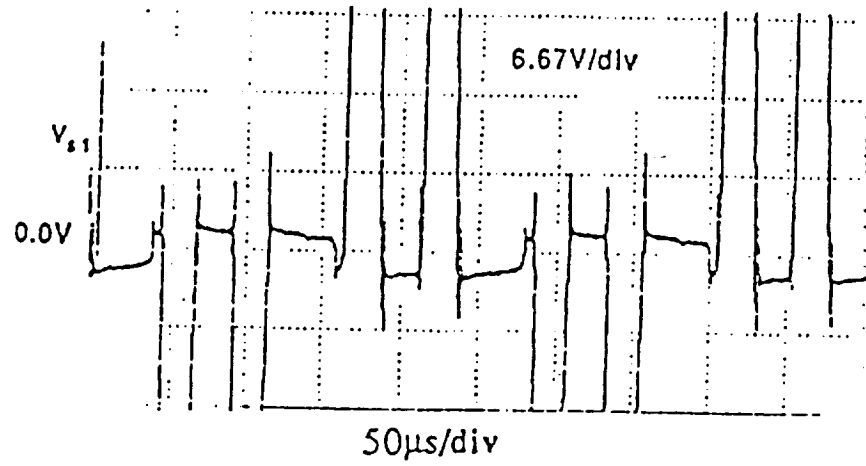


Fig. 3.18 Detail of voltage across a conducting switch.

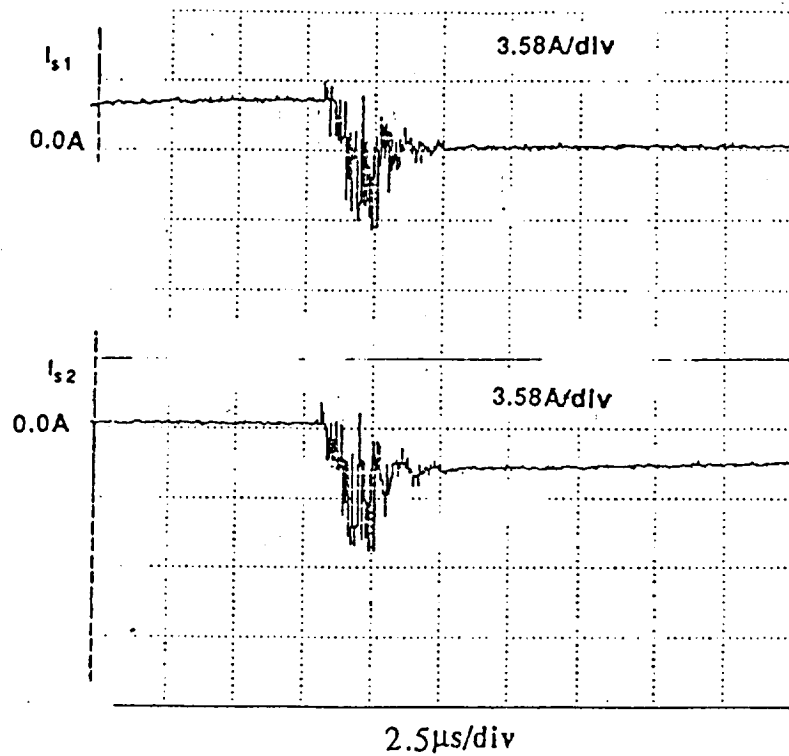


Fig 3.19 Detail of current as S1 turns off and S2 turns on

As mentioned above, the MCT is a latching device and has a problem turning on at zero voltage. However, in the zero-voltage switching experiment, the bi-directional switches were able to turn on at the zero crossings. To explain this, one should start from the structure of the bi-directional switch configuration used in this experiment. The bidirectional switch used has a back-to-back diode pair in each switch which helps turn the devices on at zero crossing.

Since only one bi-directional switch can be on at a time, the voltage across the one that is off is then at the high frequency ac link voltage, V_{ac} , and the scenario is similar to that in Fig. 3.20. The voltage drop across the switch that is on is assumed to be negligible and therefore not shown in Fig. 3.20. Note that there are two parasitic capacitors shown in the figure and they play an important role. The initial voltage across the parasitic capacitor has to be zero because this switch has been on. V_{ac} will charge one of the parasitic capacitors (through the other diode) during the first quarter cycle, then the other capacitor will be charged during the second quarter cycle. After the first half cycle, the voltage across each of the capacitors will still be sinusoidal but never cross zero voltage. The diode voltage therefore has a dc offset and the waveforms are shown in Fig. 3.21. As can be seen in Fig. 3.21, at each the zero crossing of the high frequency link, the voltages across the devices are always half of the peak of V_{ac} . In another words, the devices will be turned on at half of the peak of V_{ac} instead of at zero voltage. Therefore as soon as an MCT is turned on a parasitic capacitor is discharged. The discharge energy

$$\frac{1}{2} C_d \left(\frac{V_{ac,peak}}{2} \right)^2 \quad (3.1)$$

is, however, very small because the parasitic capacitance, C_d , is negligible.

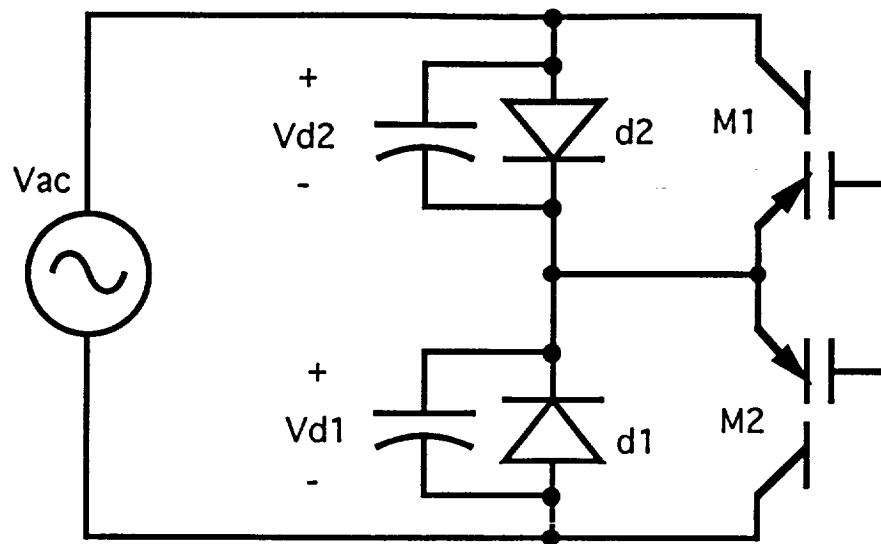


Fig. 3.20 Equivalent voltage across a bi-directional switch that is off.

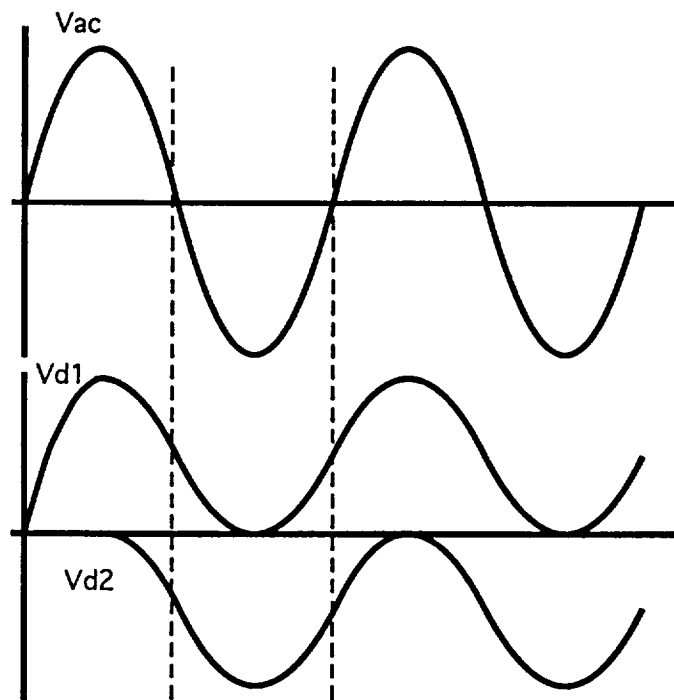


Fig. 3.21 Waveforms of ac link voltage and voltage across each device in a bi-directional switch when off.

Turn-on and turn-off failures of the device have been reported under zero voltage switching tests. In many cases, it failed at low voltage and current level compared to the rating of the device. The causes of failures are still uncertain. In an effort to investigate the failure modes, the damaged MCTs were examined.

Under normal operation in our experiment, the devices do not have any noticeable thermal dissipation, therefore, it can be concluded that thermal heating is not a cause of failure. Except for some unexplained failures, it has been noticed that a device would fail when some transient occurred in the circuit. Example transients are a step increase of the resistance in the RLC load and misinformation mixed into the control logic causing high frequency switching that does not necessarily occur at zero voltage.

Most of the damaged devices measured finite resistance of about 20Ω to 30Ω between gate to anode which seems to imply damage to the "MOS" part of the MCT. Some of the damaged MCTs were still able to switch and block voltages below $\approx 30V$. This, however, differs from case to case.

Since the damaged devices were still able to switch, often the failure could not be detected until a high current drawn by the gate drive circuit was observed. When an MCT failed, the negative gate drive current went lower when the devices were switching. Under these conditions it is believed that part of the anode current flowed into the gate while the device was conducting.

CHAPTER IV

SNUBBER CIRCUITS FOR MCTS IN AN AC/AC PDM CONVERTER

4.1 INTRODUCTION

Conventional power conversions involve mechanically coupling systems. For example, an ac/dc conversion requires ac and dc motors with one driving the other. The mechanical movements often cause significant power losses, not to mention their physical sizes and weights. One attractive feature of power electronics is very low power losses compared to the conventional power conversions methods. With sufficient maintenance (especially on a dc motor), the conventional system is fairly reliable. On the other hand, the reliability of a power electronics system depends mainly on the power devices being used. In order to guarantee the dependability of a power device, there are a few things one should pay attention to: (1) the device's maximum current, voltage and thermal dissipation ratings, known as the safe operating area (SOA) of the device, (2) possible faults of the circuit like shoot-through current, voltage spikes, etc. To reduce faults and protect the device, snubber circuits are used.

A snubber cannot reduce the total power losses (and most of the times it even increases the total power losses) but it reduces the device power dissipation and maintains the device within its SOA. Two kinds of snubbers used in ac and dc power conversions will be discussed in the later sections

4.2 Snubber Circuits For Dc Bi-Directional Switches

The basics of turn-on and turn-off snubber circuits can be found in most power electronics text books. In this chapter we concentrate on snubber circuits for

MCTs. As found in the hard switching experiment in Chapter Three, turn-on of MCTs is instantaneous and does not dissipate significant power by observation. What could cause the device to operate out of the SOA is the current tail during turn-off. This current tail at turn-off will in turn increase thermal dissipation and thus create a longer tail. If not corrected, this problem will eventually make the MCT “run away” and become damaged. Therefore, the suggested protecting device for an MCT is a turn-off snubber.

There are two kinds of turn-off snubber circuits, one is dissipative and the other is non-dissipative. They both limit the rate of change of anode-to-cathode voltage, $\frac{dV_{AK}}{dt}$ at turn-off. Consider the circuit shown earlier in Fig. 3.4. As the MCT is switched off, it becomes a high impedance path and, therefore, all the inductor current is assumed to pass through the snubber capacitor and diode. Before turn-off, the snubber capacitor voltage is equal to V_{dc} . The freewheeling diode will not turn-on until the snubber capacitor voltage is discharged to zero. Therefore, before the freewheeling diode turns on, the current through the capacitor is I_{load} and can be described as:

$$C_s \frac{d}{dt} V_C = -I_{load} \quad (4.1)$$

by integrating both sides gives

$$V_C(t) = V_{dc} - \frac{I_{load}}{C_s} * t \quad (4.2)$$

and since

$$V_{AK} = V_{dc} - V_C(t) \quad (4.3)$$

combining (4.2) & (4.3) gives

$$V_{AK} = \frac{I_{load}}{C_s} * t \quad (4.4)$$

Figure 4.1 shows graphically how the snubber circuits reduce the power dissipation by decreasing dV_{AK}/dt at turn-off.

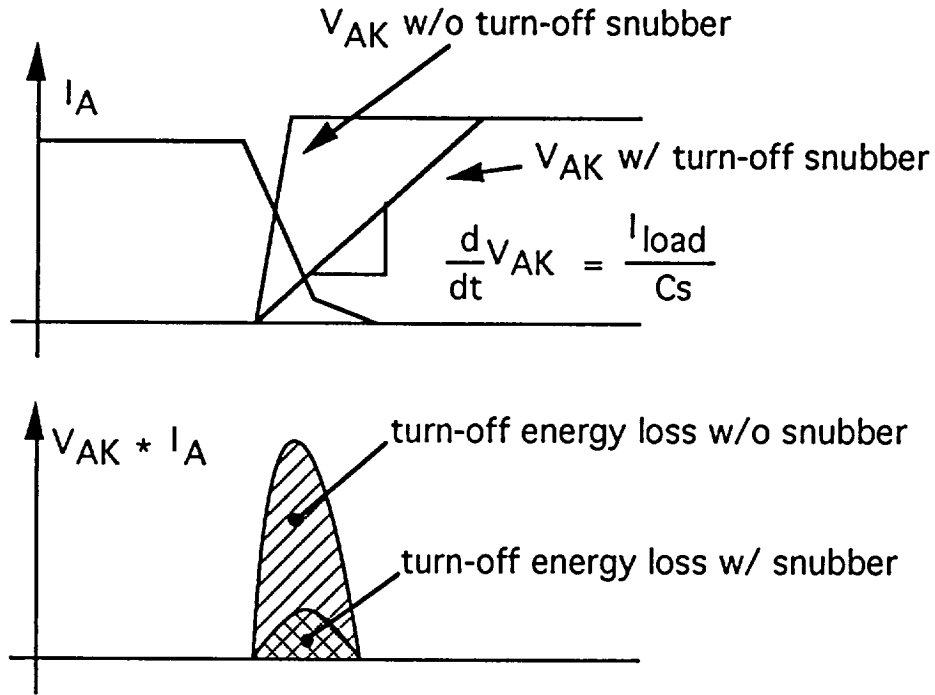


Fig. 4.1 A sketch of anode current I_A and anode-to-cathode voltage V_{AK} during turn-off with and without snubber circuits. And comparison of power losses

The snubber capacitor will be charged to V_{dc} through the resistor when the MCT is turned on. The energy dissipated in the resistor, E_r , is equal to the energy stored in the capacitor, E_c , and are given by

$$E_r = E_c = \frac{1}{2} C_s * V_{dc}^2 \quad (4.5)$$

The energy dissipated in the resistor is unrecoverable and therefore all contribute to loss. The losses due to the snubber circuit (P_{loss}) at the switching frequency, f_{sw} , is

$$P_{loss} = E_r * f_{sw} \quad (4.6)$$

The power loss in the snubber circuit and the increase in turn-off time are considered as disadvantages of this kind of snubber circuit. If recovery of the power is important, a non-dissipative snubber, as shown in Fig. 4.2, can be used to replace the dissipative snubber. There is no dissipative element, like a resistor, in this circuit. The operation of this snubber when placed across the free wheeling diode of Fig. 3.4 is similar to the dissipative snubber but now the load current discharges two capacitors at turn-off instead of one. At turn-on the dc voltage source, charges two capacitors and one inductor in series without dissipating any power. However more components and larger sizes are required in a energy recovery snubber circuit. If losses of power due to the snubber circuit is not significant, it is better just to use the dissipative snubber.

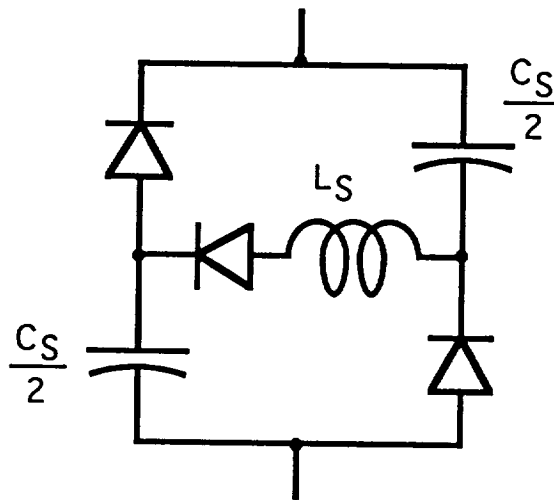


Fig. 4.2 A non-dissipative turn-off snubber circuit. This is connected in parallel with the free wheeling diode.

4.3. Snubber Circuit for Ac Link Bidirectional Switches

As mentioned in Chapter One, the PDM converter takes advantage of switching an MCT at zero voltage and thus minimizing turn-on and -off losses. It is not necessary

to further reduce the switching losses by using snubber circuits. The reasons for needing a snubber in this case are different than those in the dc chopper.

In an ac/ac PDM converter with inductive load, there are two possible faults that may cause damage to the devices: 1) an instant of open circuit ,2) short circuit. Due to the fast switching capability of MCTs, the fault could occur due to delays of turn-on, turn-off or control of the gate-drive. In such situations soft switching will not be achieved. Consider the simplified ac/ac PDM converter shown in Fig. 4.3 in which each switch, S1 or S2, consists of two diodes and two MCTs. For example, a turn-on delay of an oncoming switch causes a high impedance path for an inductive load. Therefore high voltage spikes will appear across both switches S1 and S2 during that time.

The possible fault mentioned above will normally not happen in most of other converters or inverters such as a pulse width modulation (PWM) inverter where freewheeling diodes can always pick up the load current even when all the switching devices are off.

The shoot-through current fault, is more of a concern in other power electronic circuits. It is basically caused by a small turn-off delay in the off-going switch, therefore there is a small instant when both switches are on and will short the voltage source. In an ac/ac PDM converter this shoot through current is definitely smaller than in a PWM inverter for the switches short a voltage around zero volts instead of shorting the dc link in a PWM inverter. However in a 20kHz ac/ac PDM converter, if the delay is $1.5\mu\text{s}$ and the peak of the ac link, V_{ac} , is 400V, with some simple trigonometry calculation it is found that the switches are shorting $\approx 75\text{V}$ and still very possibly cause high shoot through current. Since the source voltage is ac, this current spike can either be positive or negative, this converter requires a snubber that can protect $\frac{di}{dt}$ in both polarities. Conventional solutions to this problem include delaying the turn-on time of the oncoming switch and connecting an inductor-diode pair in series

with the switches. Due to the nature of ac/ac PDM converters such as the bidirectional conduction requirement, these solutions cannot apply to this problem.

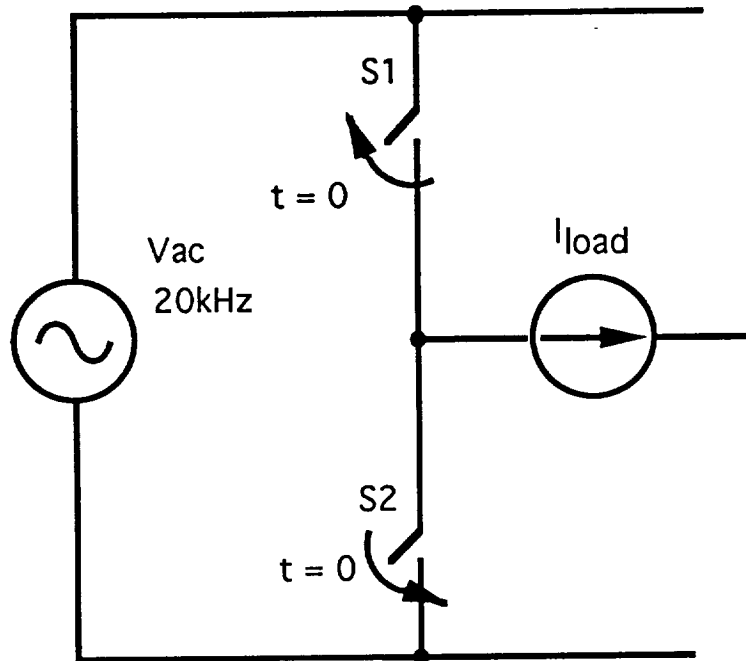


Fig. 4.3 An ac/ac PDM converter with simplified switches, S1 and S2 shown. Each switches consist of two MCTs and Two diodes.

Theoretically, only an ideal case can guarantee soft switching. The ideal case occurs when the turn-on of one switch and turn-off of the other happens simultaneously at $t=0$, as shown in Fig. 4.3. A possible method to achieve this is to compensate the known delays for turn-on and turn-off times accurately at the expense of complicating the control and drive circuits. Unfortunately, the turn-on and turn-off delay times can change as current and/or voltage levels varies, thus making accurate compensations unfeasible. There is a need for a snubber circuit that can still maintain soft switching under non-ideal conditions. In the following paragraphs, different snubber circuits for different cases will be considered.

Case I Perfect Switching Timing (Fig. 4.3): As said earlier, under perfect switching timing (Fig. 4.3) and zero-crossing switching, an ac/ac PDM converter has

negligible losses and a limited $\frac{dv}{dt}$ in the devices. Even when there is current tail at turn-off, under perfect switching timing, the losses in the device are still small compared to that of other power converters. Therefore, a snubber circuit is not necessary.

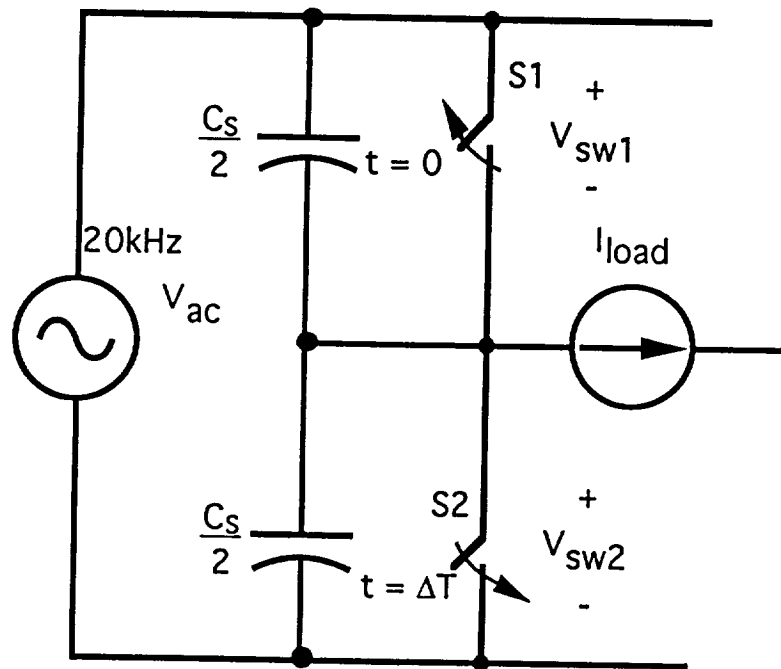


Fig. 4.4 A turn-on delay of ΔT in S2 causes an instant of open circuit for the current source load. Two snubber capacitors are used to keep the current continuous and reduce voltage spike across the devices.

Case II A turn-on delay of ΔT in the oncoming switch(Fig. 4.4): In this case, the switches are both off for a time period of ΔT . The off state impedance of the switches is very high and the inductive load current has to continue during this time, thus a voltage spike will appear across each switch. The magnitude of this voltage spike depends mainly on the parasitic capacitance of the devices. Since this capacitance is very small, the voltage spike will be so high and can damage the MCTs.

With two snubber capacitors connected as shown in Fig. 4.4, the voltage spike magnitude can be limited. The maximum possible value of the voltage across each

switch, V_{sw} can be obtained by superposition of two voltages; one due to the ac source and the other due to the load current:

$$|V_{sw}(\Delta T)| = \left| \frac{V_{ac}(\Delta T)}{2} \right| + \left| \frac{I_{load} * \Delta T}{C_s} \right| \quad (4.7)$$

therefore

$$\frac{C_s}{2} = \frac{|I_{load} * \Delta T|}{|V_{sw}(\Delta T)| - \left| \frac{V_{ac}(\Delta T)}{2} \right|} \quad (4.8)$$

since ΔT is very small compared to a cycle of V_{ac} , thus

$$V_{ac}(\Delta T) \approx \left[\frac{dV_{ac}}{dt} \right]_{t=0} * \Delta T \quad (4.9)$$

and at 20kHz

$$V_{ac}(\Delta T) = 2\pi (20 * 10^3)^3 * V_{ac,peak} * \Delta T \quad (4.10)$$

Let $V_{ac,peak}$ be 500V. If the maximum allowable voltage spike, load current and possible turn-on delay are 400V, 20A and $1\mu s$ respectively, then, using equations (4.7)-(4.10), the required snubber capacitance will be $0.03\mu F$. Figure 4.5 shows the transient voltage across each switch, V_{sw} .

Although the voltage spikes are limited to a permitted value, it can still cause another problem. When the oncoming switch starts to turn-on at ΔT , it will short a capacitor that has just been charged to 400V in the worst case. This discharging current is unbounded and its rate of increase, $\frac{di}{dt}$, is limited only by the lead inductance. This can damage the device in many cases.

The dc chopper, in the previous section, has a snubber capacitor which is connected in series with a resistor-diode pair so that the charging (or sometimes discharging) current is limited. In fact, a similar snubber can still be used in the bidirectional switches like that in Fig. 4.6. This snubber circuit needs two resistors,

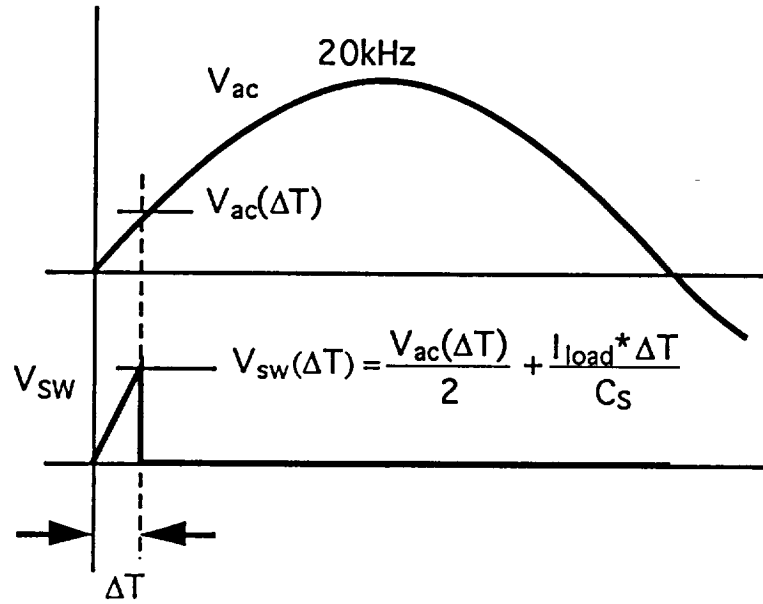


Fig. 4.5 Graphical representation of ac link voltage, V_{ac} , and the voltage across each switch during ΔT the turn-on delay.

two diodes and one more capacitor. By using the same analysis on the single capacitor snubber, it is found that for every cycle of V_{ac} , at least one of the capacitors will be charged to the peak of V_{ac} . Energy losses in this snubber circuit are much higher than the one with a single capacitor on each bi-directional switch. A better way of limiting this discharging current will be presented later in this Chapter.

For most devices, a large discharge current is considered damaging. However, whether this will damage an MCT is questionable because an MCT has a thyristor structure which can handle high current density and $\frac{di}{dt}$. A recent study on MCTs suggested that "the high $\frac{di}{dt}$ and good hard turn-on capability allows use of a snubber consisting of a capacitor alone, reducing snubber cost and simplifying the circuit"[9]. The maximum stored charge, $C_s * V_{C_s}$, that the MCT can discharge is, however, not specified in [9]. Even if it is safe to use a capacitor snubber alone when used with MCTs, there is still another disadvantage of this snubber is that it cannot protect the devices from shoot-through current due to an instant of short circuit.

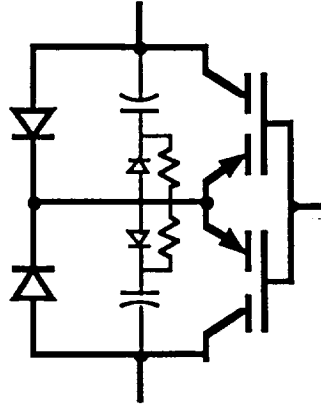


Fig. 4.6 Ordinary turn-off snubbers used in a Bidirectional switch

Case III A turn-off delay of ΔT in the off-going switch: Note that from Equation (4.10), at 20kHz, one microsecond after zero crossing the voltage rises up to $1/8$ of $V_{ac,peak}$, $\approx 63V$ for example. If there is a one microsecond delay in the off-going switch, the devices will be shorting the voltage source from 63V to 0V. the current through the devices might rise unboundedly. Whether the current will shoot-through depends on how ideal the ac source is. The ac source being used is just the output of a Mapham inverter which is not an ideal source. When the source is shorted at zero voltage, the currents and rate of change of currents through S1 and S2 can actually be limited by either one of the resonant inductors, L_{r1} or L_{r2} , as shown in Fig. 4.7. Therefore this fault will only delay a resonant cycle by ΔT as shown in Fig. 4.8. It can be seen that soft switching is still maintained.

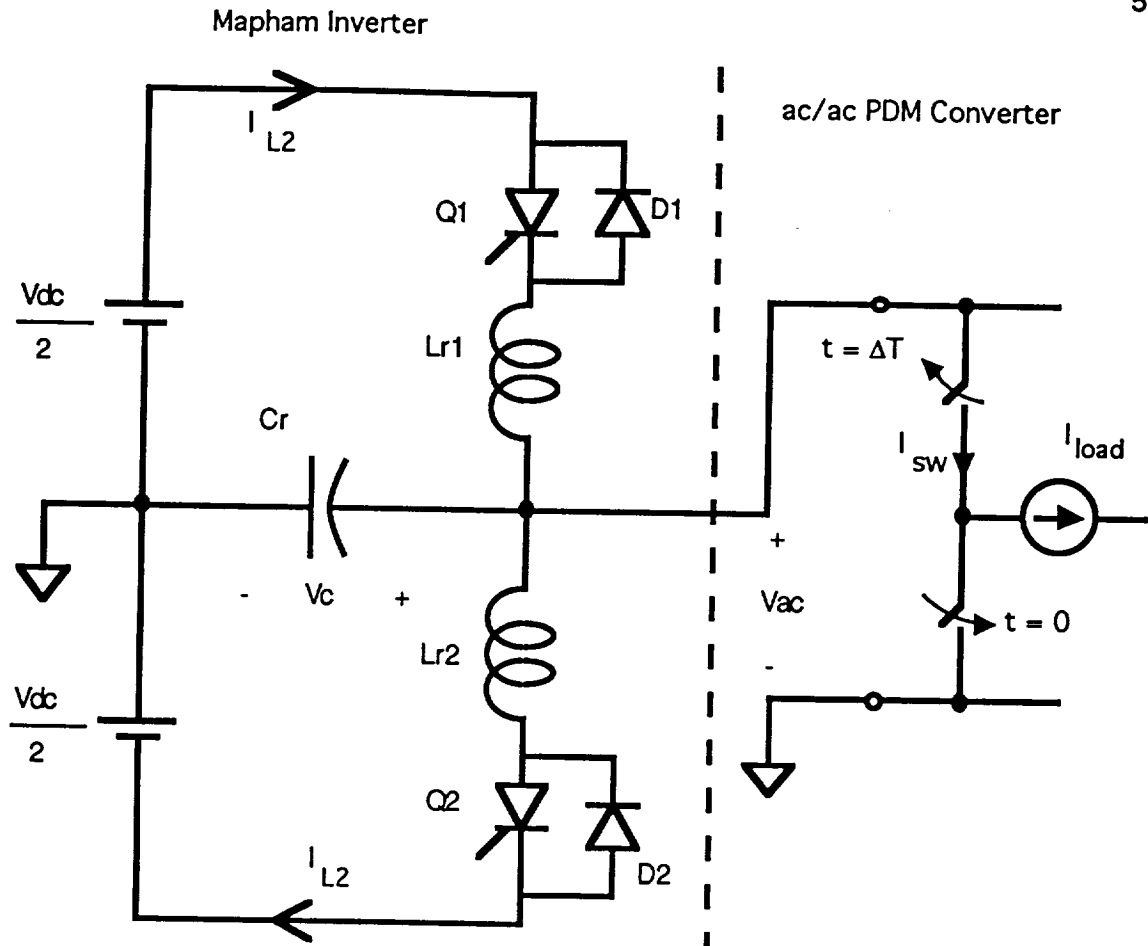


Fig. 4.7 An PDM converter with a Mapham inverter as a voltage source.

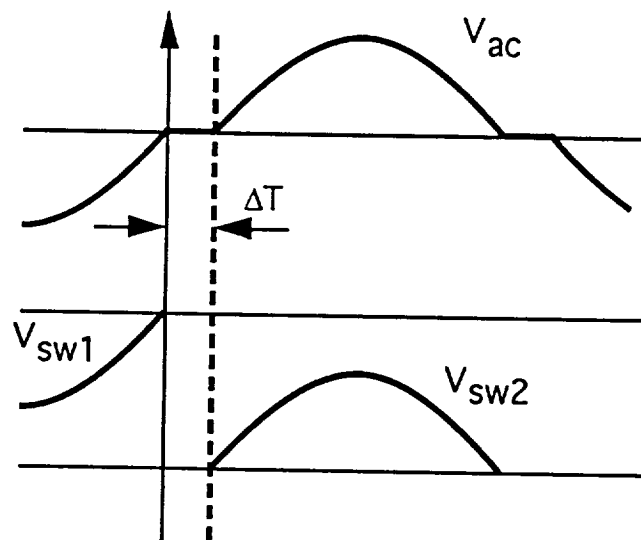


Fig. 4.8 An example waveforms of voltages across the ac link and the switches during an instant of short-circuit across the ac source.

Although an instant short-circuit fault at zero voltage will not cause problem if the ac link voltage source is a resonant inverter, in the original interest of this research, a stiff voltage source is assumed and needs to be considered. The following discussions is about the possible shoot-through current caused by shorting an ideal ac link source.

Figure 4.9 shows a PDM converter with a snubber inductor in series with each switch. The purpose of these snubber inductors is to limit the shoot through current due to a short circuit. The sizes of these inductors can be determined by expressing the switch current in S1 and S2 as:

$$i_{sw}(\Delta T) = \frac{1}{L_s} \int_0^{\Delta T} V_{ac}(t) dt \quad (4.11)$$

Note that equation (4.11) expresses only the shoot through current without taking the load current into account.

Equation (4.11) can be modified geometrically to

$$i_{sw}(\Delta T) = \frac{1}{L_s} \text{area}(0, V_{ac}(\Delta T), \Delta T) \quad (4.12)$$

where $\text{area}(0, V_{ac}(\Delta T), \Delta T)$ is defined in Fig. 4.10. The area under V_{ac} from 0 to ΔT can be approximated, for small ΔT , by

$$\text{area}(0, V_{ac}(\Delta T), \Delta T) \approx \frac{1}{2} V_{ac}(\Delta T) * \Delta T \quad (4.13)$$

Hence using Equation (4.9) - (4.13), the shoot through current at 20kHz is

$$i_{sw}(\Delta T) = \frac{10 \cdot 10^3 \pi * V_{ac,peak} * \Delta T^2}{L_s} \quad (4.14)$$

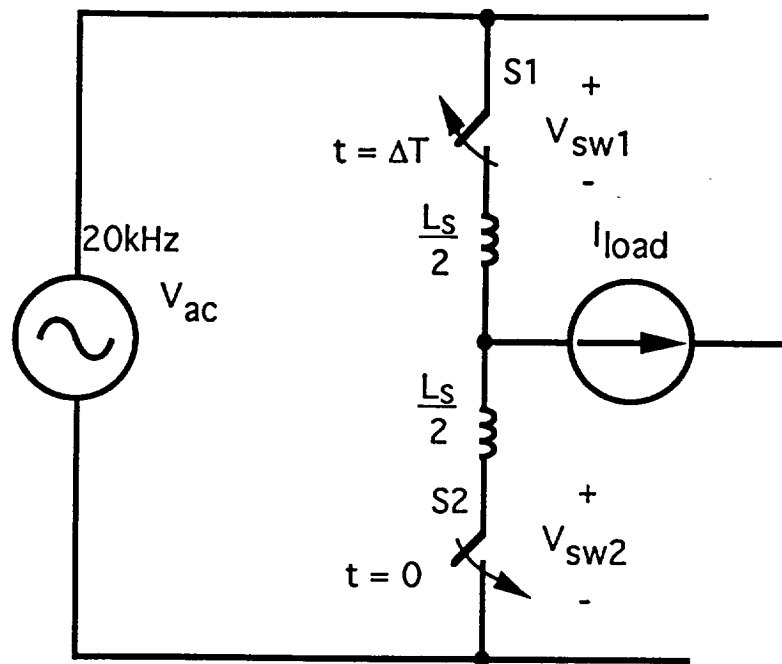


Fig. 4.9 A turn-off delay of ΔT in S1 causes an instant of short circuit for the voltage source. Two snubber inductors are used to limit the shoot through current.

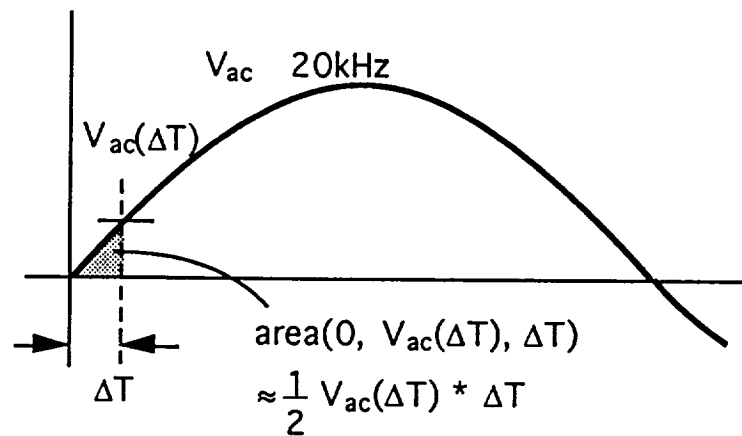


Fig. 4.10 For small ΔT the area under the sinewave can be approximated by a triangle.

An interesting result from Equation (4.14) is that it does not need much inductance to limit $i_{sw}(\Delta T)$ and $\frac{di_{sw}(\Delta T)}{dt}$. As an example, using the same parameter from the previous case, i.e. $\Delta T = 1\mu s$ and now the maximum permitted shoot-through current, $i_{sw}(\Delta T)$, due to this fault = 10A, it is found that $\frac{L_s}{2}$ needs to be as small as

only 0.78 μ H. Also, $\frac{di_{sw}(\Delta T)}{dt}$ is limited to 80.6A/ μ s which is far below the maximum rating of the MCT (5000A/ μ s).

Since current in the snubber inductor has to continue, a free wheeling diode is connected in parallel with the inductor to avoid voltage spike caused by the sudden change of current at turn-off. The snubber inductor and the freewheeling diode in a bi-directional switch should be placed as shown in Fig. 4.11 so that the current always flow in one direction however the direction of the current of the switch is. The free wheeling diode, d_{fw} , can always pick up the inductor current when the devices are off. It is known from the above analysis, the size of this inductor is much less than a few microhenrys and therefore it will not be too bulky for the circuit.

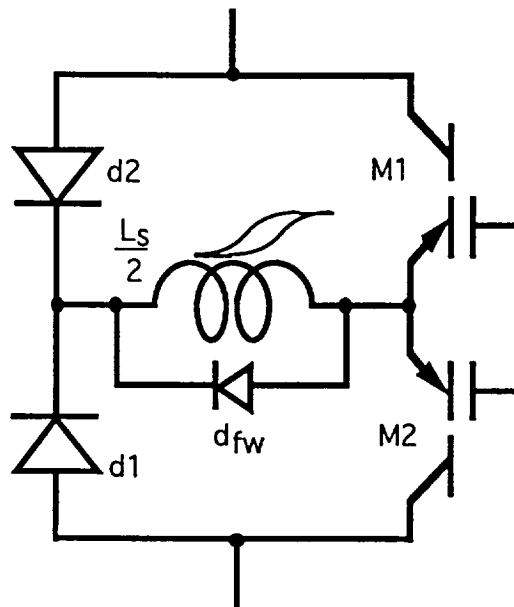


Fig. 4.11 The best location of the snubber inductor and free wheeling diode in each bidirectional switch.

Note that there is an advantage of using saturable inductor snubbers in this case. First of all, the purpose of this inductor is to limit the possible shoot through current caused by an instant of short-circuit at switching. When the switch is already conducting current, the snubber is, in fact, not needed. A saturable inductor can provide

the required inductance when the switch is just turned on. After the current passes the saturation level, the inductance of the snubber becomes negligible and invisible to other parts of the circuit. The energy stored by the saturable inductor is limited and causes only a small voltage drop. Thus it has a small influence on the other parts above the saturation level. Usually a saturable core has high permeability and needs only a few turns to provide the required inductance for the snubber circuit so that it does not occupy much space. Since the inductor stores only small energy, the free wheeling diode, d_{fw} , can discharge the snubber inductor current to zero through its on-voltage during the off cycle of the switch. Thus, the snubber can always start with zero initial current.

The inductive snubber is, in fact, this snubber is the dual of the capacitive snubber. The disadvantages of the snubber are also the dual of that of the capacitive snubber. It cannot protect the device from voltage spikes that caused by an instant of open circuit. It can even cause voltage spikes due to a step change in the snubber inductor current when the device is just turned on. A combination of both inductive and capacitive snubbers may solve the possible problems associated with both snubbers used alone and the faults discussed in cases I and II. The proposed snubber is shown in Fig. 4.12, which combines the features of both capacitive and inductive snubber circuits. The analysis for the proposed snubber circuit is more complicated than of each the individual snubbers. The purpose of the capacitor is to limit the voltage spikes across the devices at switching. The inductor limits the inrush current through the devices at switching.

4.4 Analysis of The Proposed Snubber Circuit

A simplified circuit diagram of the proposed snubber circuit is shown in Fig. 4.13. As can be seen in Fig. 4.13, the snubber circuit itself is a resonant circuit which, again, takes advantages of soft changes of resonating voltage and current. The snubber

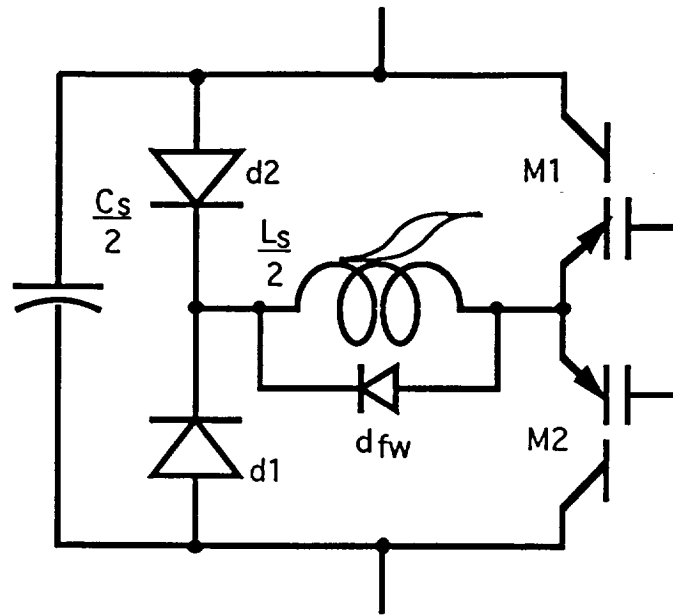


Fig. 4.12 Proposed snubber for the by directional switch which combines the features of both capacitive and inductive snubbers.

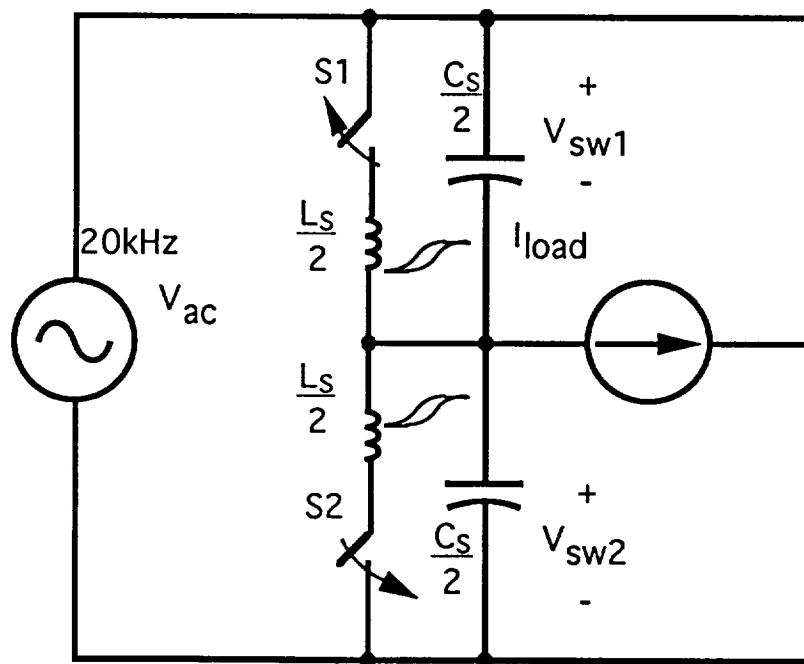


Fig. 4.13 Simplified ac/ac PDM converter with proposed snubber circuit. Each snubber inductor has a free wheeling diode (not shown) in parallel so no voltage spike occurs across the devices at turn-off.

inductors are also saturable because inductance is needed only when a switch is closed so that the rate of change of current is limited. Since this snubber circuit consists of a non-linear inductor, accurate quantitative calculations of resonance with the non-linearity are tedious, a qualitative analysis is presented in the following.

Consider the two quasi-resonant circuits shown in Figs. 4.14 and 4.15. Each circuit consists of an ideal capacitor, an ideal inductor and a diode with finite on-voltage drop. In Fig. 4.14, a step current, I_o , flows into the LC circuit at $t=0$. The diode is reverse biased until the capacitor voltage reaches the on-voltage drop of the diode. From a simple second order circuit analysis, the capacitor voltage and inductor current of Fig. 4.14 can be found as

$$V_c(t) = I_o * \sqrt{\frac{L}{C}} * \sin(\omega t) \quad (4.15a)$$

$$I_L(t) = I_o * (1 - \cos(\omega t)) \quad (4.15b)$$

where

$$\omega = \frac{1}{\sqrt{LC}} \quad (4.15c)$$

However, Equation 4.15 describes the voltage and current only before the capacitor voltage forward biases the diode, because when the diode turns on it clips the capacitor voltage and discharges the inductor through its on voltage drop, V_{don} . The rate of change of the inductor current can be expressed as

$$\frac{di_L}{dt} = - \frac{V_{don}}{L} \quad (4.16)$$

The waveforms of voltage and current are described in Fig. 4.14.

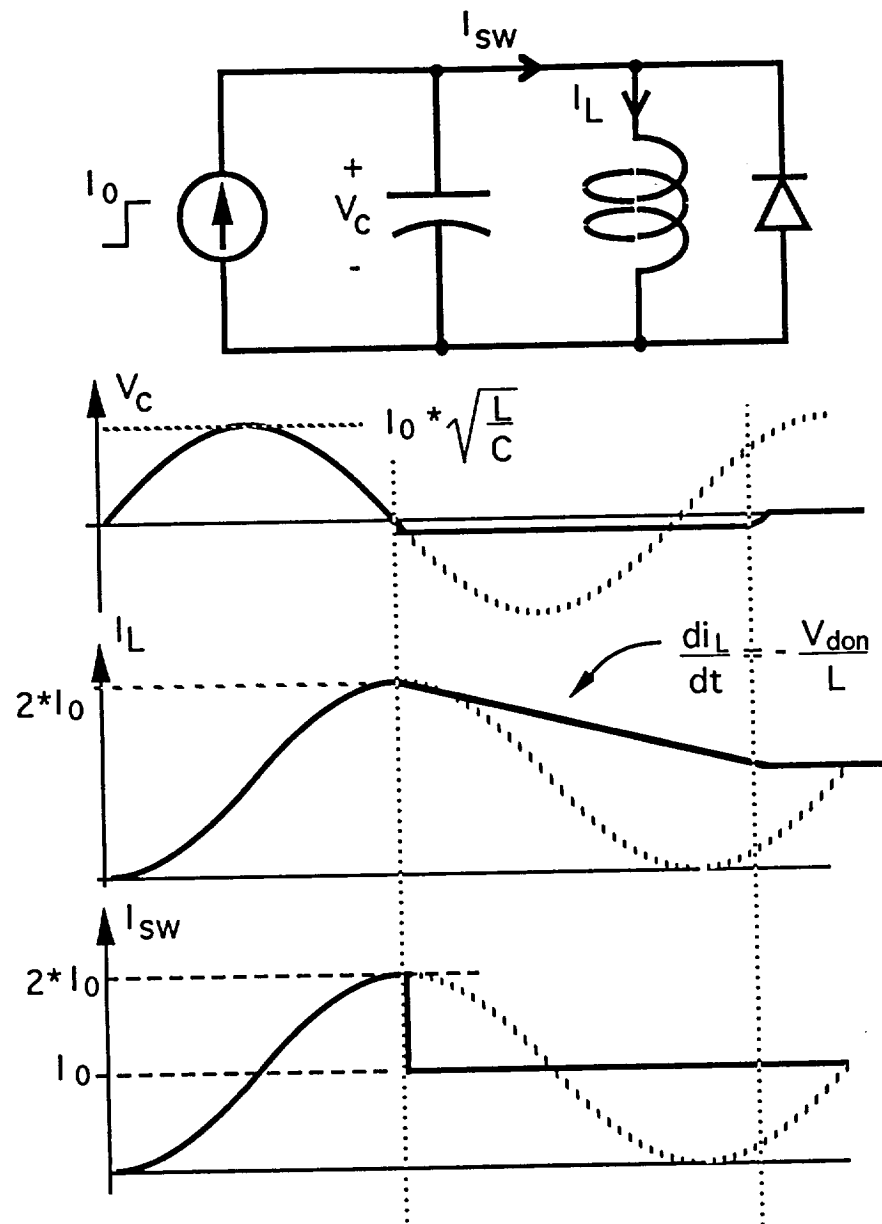


Fig. 4.14 Voltage and current response for a step current input to a parallel LC and diode circuit.

To better represent the behavior of the snubber the circuit of Fig. 4.14 needs to be modified as seen in Fig. 4.15. In Fig. 4.15, a switch is added to the circuit shown in Fig. 4.14. The switch is turned on at $t = \Delta T$. Before the switch is turned on the capacitor is charged to some initial voltage, $V_C(\Delta T)$ and can be found as

$$V_{sw,peak} = V_c(\Delta T) = \frac{I_o * \Delta T}{C} \quad (4.16)$$

During this time the diode is reverse biased it is a linear circuit, therefore superposition applies. The resulting voltage and current can be found easily by adding results due to I_o and the initial voltage of the capacitor $V_c(\Delta T)$. Using a simple second order analysis, the capacitor voltage is

$$V_c(t) = I_o \sqrt{\frac{L}{C}} \sin(\omega t) + V_c(\Delta T) \cos(\omega t) \quad (4.17a)$$

$$= I_o \sqrt{\frac{L}{C}} \sin(\omega t) + \frac{I_o * \Delta T}{C} \cos(\omega t) \quad (4.17b)$$

$$= I_o \left(\sqrt{\frac{L}{C} + \left(\frac{\Delta T}{C}\right)^2} \sin(\omega t + \phi_1) \right) \quad (4.17c)$$

where

$$\phi_1 = \tan^{-1}\left(\frac{\sqrt{LC}}{\Delta T}\right) \quad (4.17d)$$

and the inductor current is

$$I_L(t) = I_o (1 - \cos(\omega t)) + \frac{V_c(\Delta T)}{\sqrt{\frac{L}{C}}} \sin(\omega t) \quad (4.18a)$$

$$= I_o (1 - \cos(\omega t)) + \frac{I_o * \Delta T}{\sqrt{LC}} \sin(\omega t) \quad (4.18b)$$

Using phasors and simple trigonometry, Equation (4.18b) can be simplified to :

$$I_L(t) = I_o \left(1 + \sqrt{1 + \left(\frac{\Delta T}{\sqrt{LC}}\right)^2} \sin(\omega t + \phi_2) \right) \quad (4.18c)$$

where

$$\phi_2 = -\tan^{-1}\left(\frac{\Delta T}{\sqrt{LC}}\right) \quad (4.18d)$$

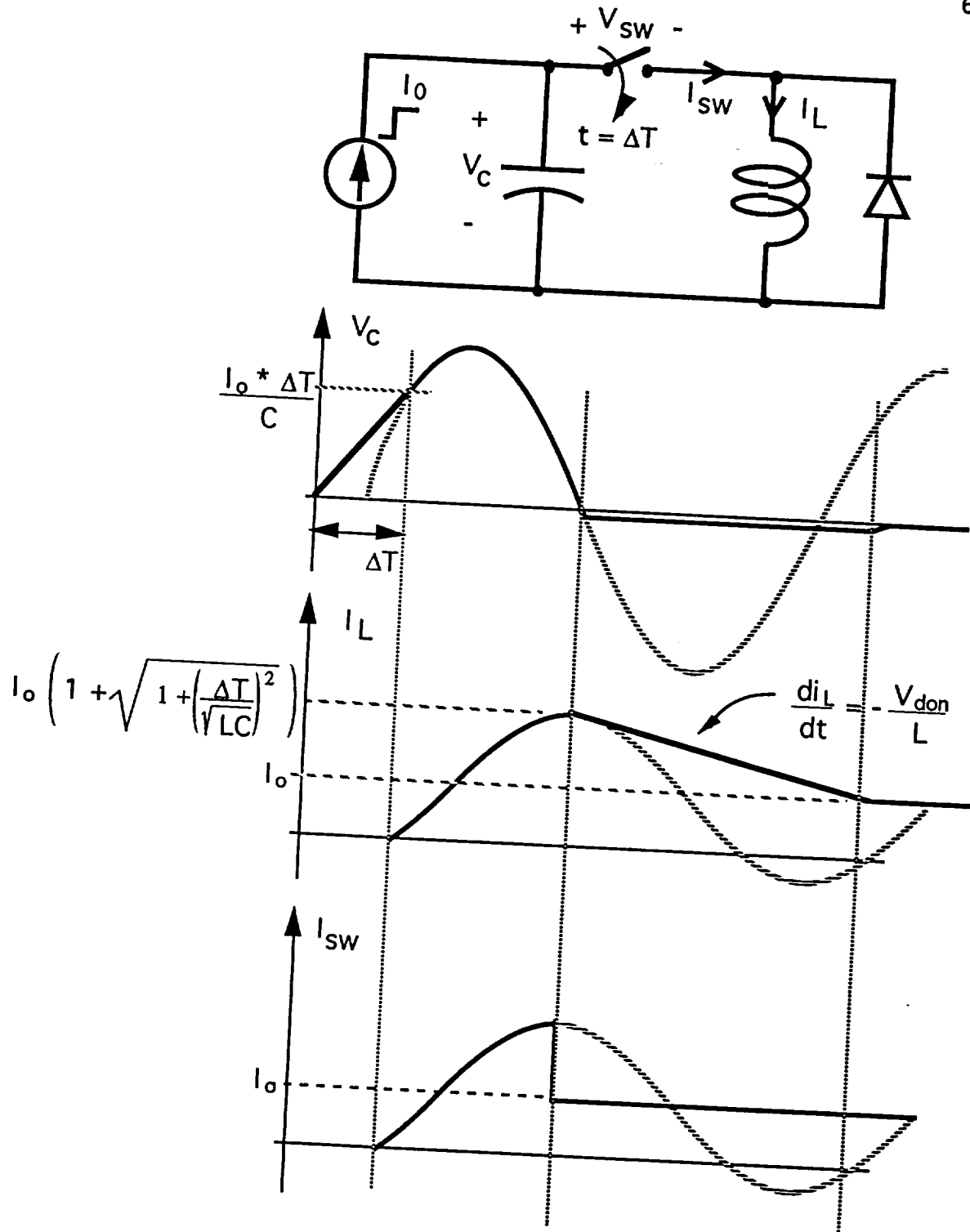


Fig. 4.15 Voltage and current responds as a current step inputs to a parallel LC and diode circuit with the switch has a turn-on delay of ΔT .

From Equation (4.16), in case of an instant of open circuit the peak voltage across the device can be found. The maximum discharging current through the device, from Equation (4.18c), is limited to about twice as I_o for small ΔT .

The above equations are only valid before the diode turns on. Similar to other resonant circuits, the diode turns on when the capacitor voltage tries to forward bias it. Once the diode turns on, the capacitor voltage is clipped at V_{don} and Equation (4.16) describes the inductor current. Fig. 4.15 shows the idealized waveforms.

The circuits in Fig. 4.15 describes the proposed resonant type snubber in case of a turn-on delay. V_{sw} and I_{sw} are the voltage across and the current through the switching device. I_o is the load current. With this snubber circuit, the switching device is always turned on at zero current.

An LC circuit has been theoretically shown to limit the transient voltage and current to finite values. The value of the snubber capacitance, C_s , can be determined from Equation (4.16). For example, if a 200V voltage spike across the MCTs is allowed before turn-on, the maximum possible turn-on delay and load current are 1.5us and 20A respectively, then, from Equation (4.16), C_s is found to be 0.15uF. The capacitance of each snubber capacitor, $\frac{C_s}{2}$, equals to 0.075uF. In other words, when the MCT is turned on, it discharges the snubber capacitor with a worst case voltage of 200V. The discharging current is limited by the snubber inductor. In general, the snubber protects the device from dissipating high energy during a short fault time ΔT . For example, the energy stored in the snubber capacitor is not dissipate in the switching device, MCT in our case, but, instead, goes through the snubber inductor into the free wheeling diode. As the snubber inductor first absorbs energy from both the snubber capacitor and the load current, the inductor current rises from zero then passes I_o up to the peak where the diode starts to turn on and the capacitor voltage is clipped at the diode's on-voltage, V_{don} , see Fig. 4.15. The free wheeling diode discharges the inductor

until it reaches I_0 , the initial energy stored in the capacitor has gone to the diode and it can be verified by simple arithmetic.

As for the shoot through current caused by the turn-off delay, the snubber inductor should definitely be able to limit it. The snubber inductor is designed to limit the capacitor discharging current which is found higher than the shoot through current.

In general, instead of letting the switching device dissipate high energy during a short fault time such as a short circuit or open circuit, the free wheeling diode dissipates smaller energy through a longer time. The energy stored in the snubber capacitor and inductor is assumed small and the free wheeling diode should be able to dissipate the power. But if the energy is large that it may be over the rating of the diode, a resistor in series with the diode will help dissipating the energy.

Note that the snubber inductor is saturable, and, therefore, will store only limited energy as shown in Fig.4.16. Thus the free wheeling diode is not required to dissipate very high energy when the devices are off. If a non-saturable inductor were used, the stored energy would be much higher and the diode would not be able to discharge all the current.

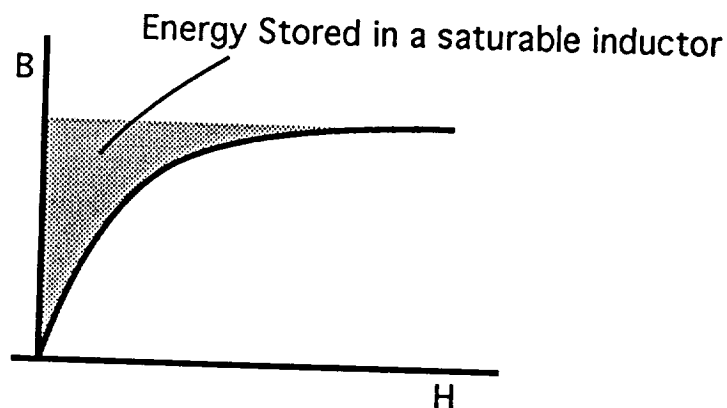


Fig. 4.16 B-H curve for a saturable inductor.

4.4 EXPERIMENTAL RESULTS

A single phase PDM converter with the proposed snubber is shown in Fig. 4.17. The low frequency current source load is implemented by connecting a series RLC circuit which has very high quality, Q , and resonates at 4kHz.

In the ideal case, when no snubber is needed, S_1 is completely on and S_2 is completely off and vice versa. This is difficult to achieve due to delays in the device

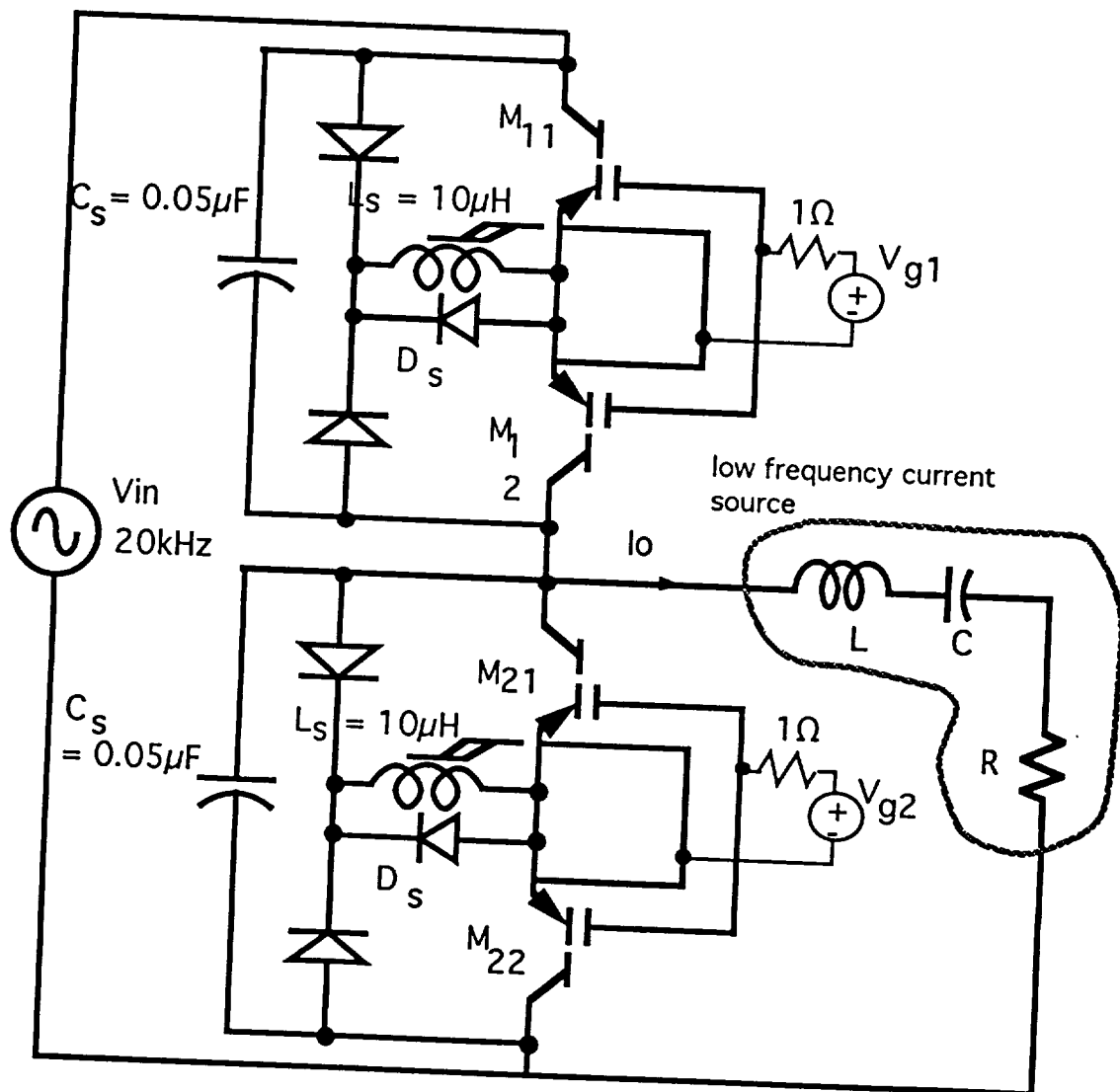


Fig. 4.17 An ac/ac converter With Proposed snubber Circuit.

itself and the drive circuit. Since it is impossible to test the device at all power levels and observe the difference in turn-on and turn-off delay, in this experiment a delay of $1\mu\text{s}$ is created intentionally by shifting the control signal of switch S1 by $1\mu\text{s}$. This causes both an open circuit and a short circuit at different edges of switching. This experiment is basically a stress test. With the fast switching characteristics of the MCT, a $1\mu\text{s}$ delay can create almost a complete open circuit at one switching edge and short-circuit at the other. The goal is to show that under this situation, with the proposed snubber circuit, soft switching is still maintained.

In this experiment, it is more important to observe the individual devices of a switch than the switch as a whole.

Without a snubber, the stress on M11 is shown in Fig. 4.18. Voltage and current spikes occur at different edges. The MCTs did survive these spikes. It was found, however, that if the voltage level was further increased misinformation was mixed into the control logic and cause random switching. Under such conditions the devices were then damaged. Therefore, the power level could not be increased without any snubbing. The misinformation was believed to be due to either the voltage spikes or the poor voltage regulation of the ac bus.

In Fig. 4.19 the voltage level was increased to a higher level than that in Fig. 4.18 without inducing misinformation into the control logic circuit because the voltage spikes are reduced significantly using only a capacitor C_s ($0.05\mu\text{F}$) as snubber. The current spikes, however, are still high. On the other hand, if the a snubber is just an inductor L_s ($10\mu\text{H}$), the current spikes are reduced (see Fig. 4.20). Again, the voltage level could not be increased due to the voltage spikes causing random switching.

When a combined capacitor and inductor snubber is used the voltage and current spikes are both reduced as shown in Fig. 4.21. As the theoretical analysis reveals, the snubber inductor slows down the rise of current through the switch and it

takes some finite time for the current spikes to come down (which depends on the on-voltage of the parallel diode). Therefore the current spikes in Fig. 4.21 is wider than those shown in Figs. 4.18-4.20. The MCT is full-on before the current spikes reach the peaks, thus the stress on the MCT is still small. Although the details cannot be shown here, from the oscilloscope it was seen that the transient voltage finishes before current starts to rise therefore soft switching is still maintained in spite of the delays. The output voltage and load current are shown in Fig. 4.22.

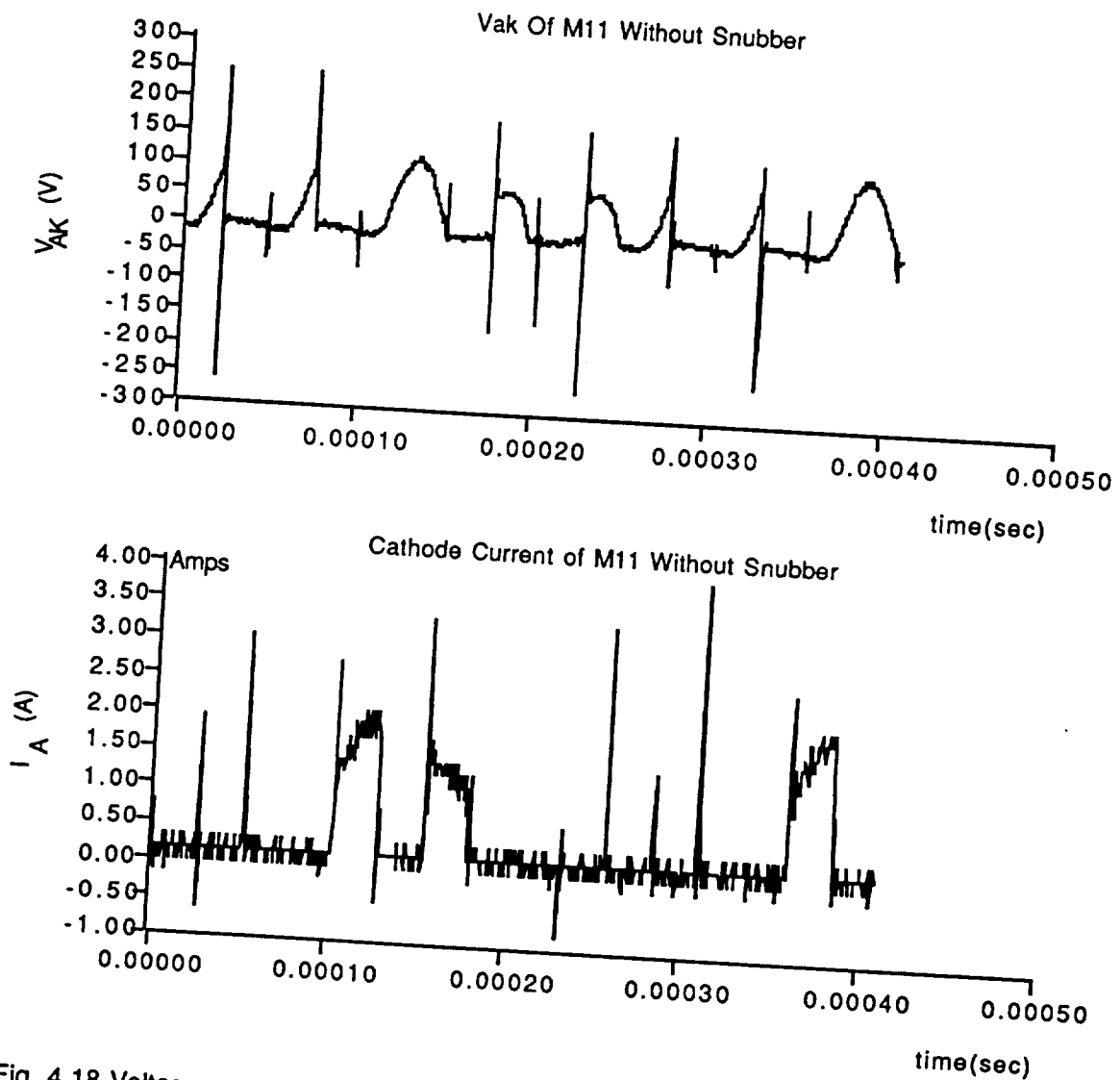


Fig. 4.18 Voltage across anode to cathode and cathode current of M11 without snubber.

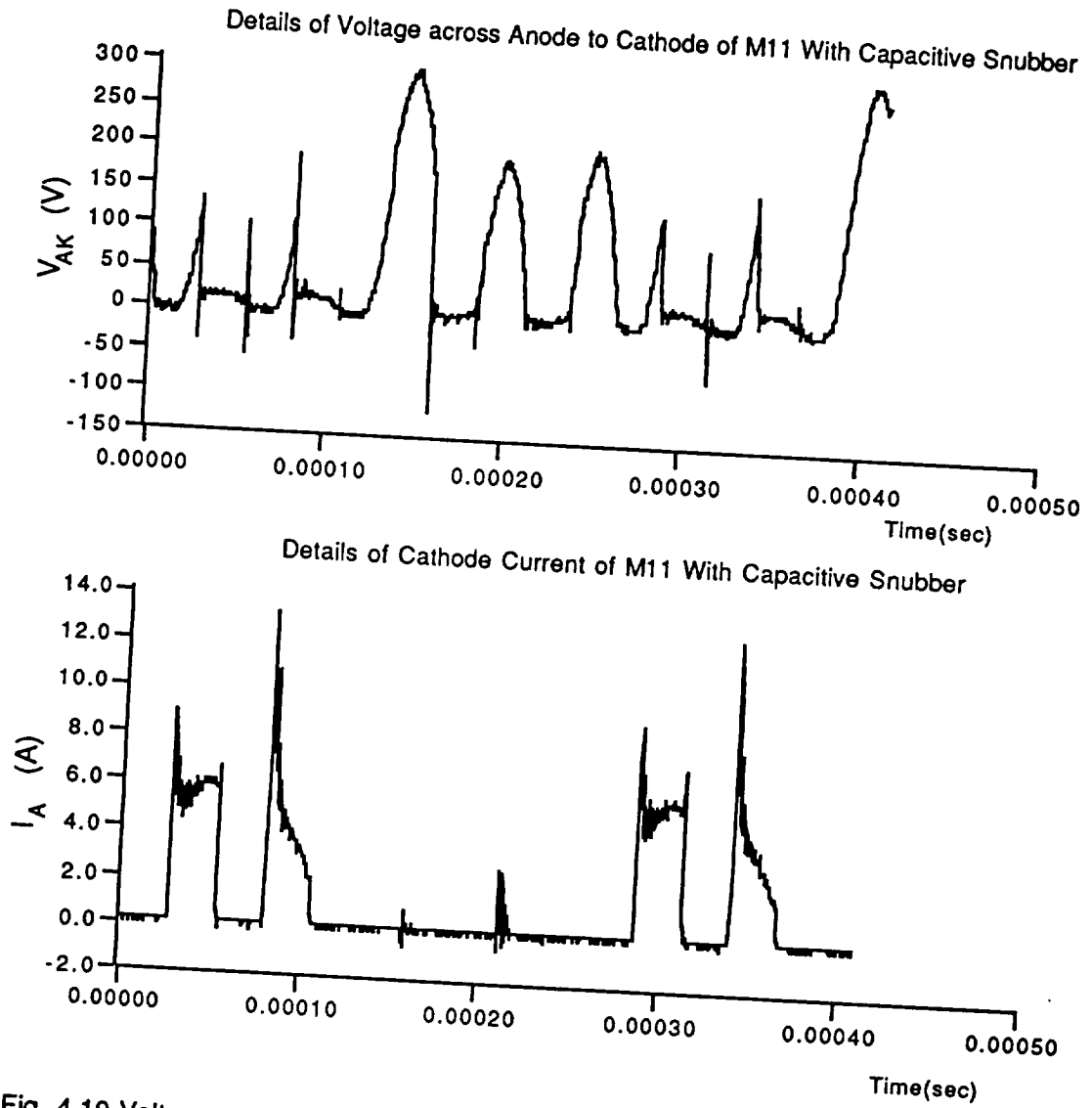


Fig. 4.19 Voltage across anode to cathode and cathode current of M11 with capacitive snubber.

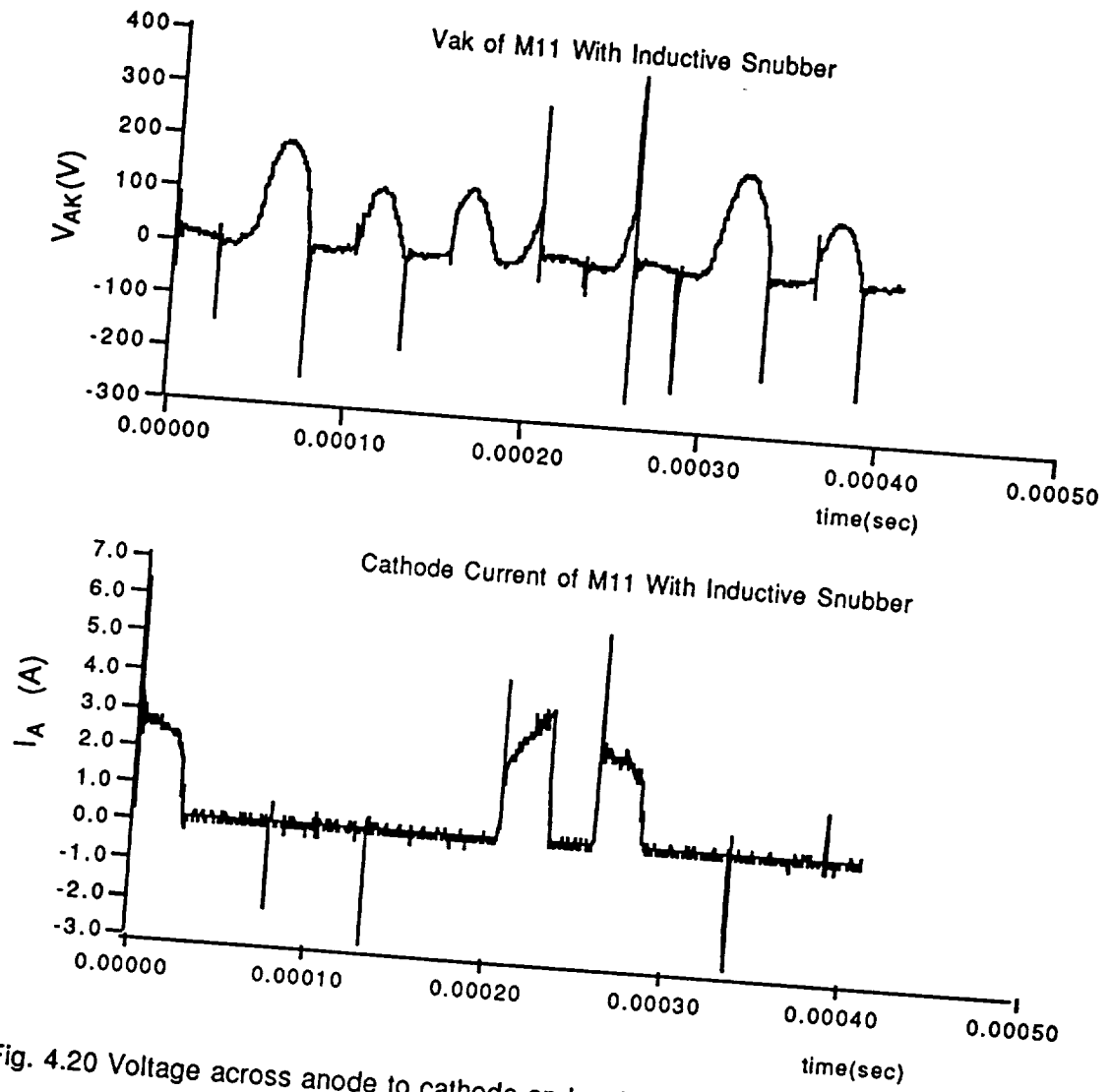


Fig. 4.20 Voltage across anode to cathode and cathode current of M11 with inductive snubber.

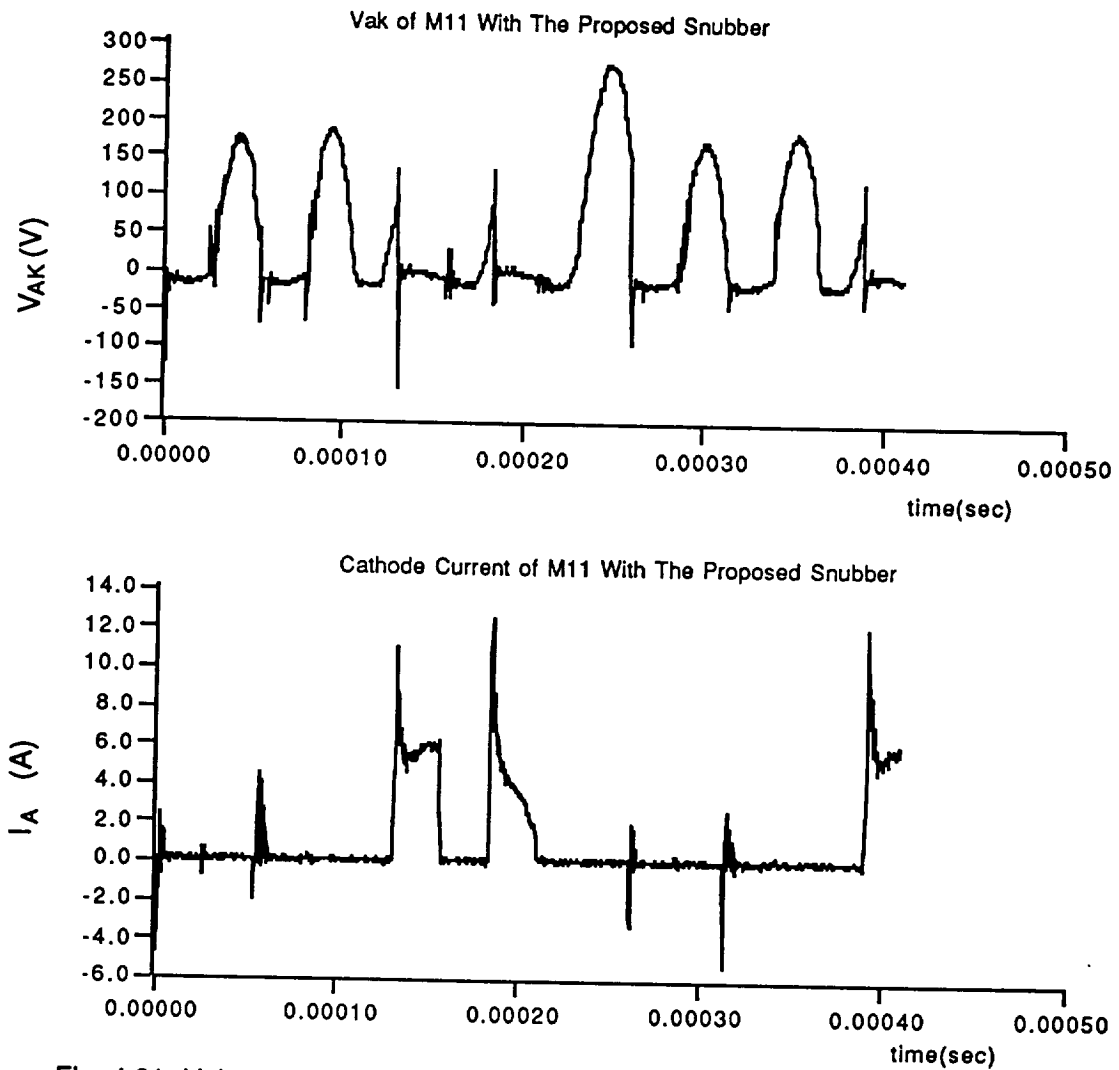


Fig. 4.21 Voltage across anode to cathode and cathode current of M11 with both capacitive and inductive snubber.

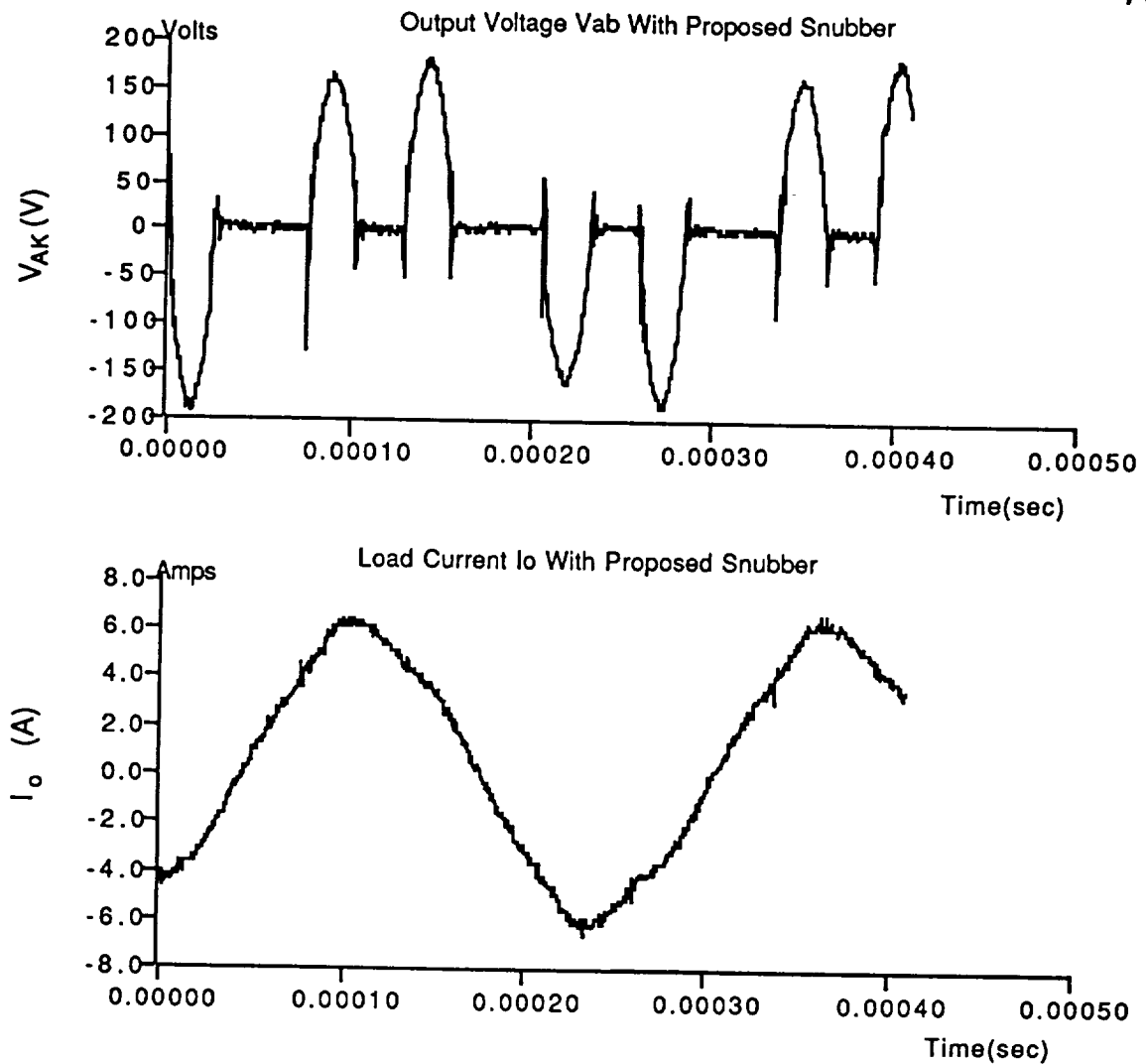


Fig. 4.22 Output voltage and load current with proposed snubber.

Anode Kelvin Current

While performing the experiments, an unexpectedly large Anode-Kelvin, I_{KEL} , current was found. The Anode-Kelvin is essentially a lead from the anode of the MCT in Fig. 4.23 used for the control signal connection. In these experiments, it was found that current circulates in the Anode-Kelvin, as shown in Fig. 4.24(b), when the devices are conducting, and this current decreases exponentially when the devices are off. As shown in Fig. 4.24, with the load current of 7A, there is a considerable fraction of current (\approx

$\frac{1}{3}$) flowing through the Anode-Kelvin. This connection, however, is supposed to only carry the gate current. This anode-Kelvin current may be the result of current division when the device is on, since the Anode-Kelvin is a fairly low resistance path. However, when the device is off, this current is decaying towards zero which is thought to be due to some parasitic capacitance discharging through the Anode-Kelvin. Whether the anode-Kelvin current will cause failures of the device is still unknown.

In summary, the MCT is a fast switching device. When connected into a bidirectional switch, it was able to be switched at zero voltage. For such a fast device, the difference between turn-on and turn-off delays has a potential problem of voltage and current stress. A generalized voltage and current snubber was found to be useful in reducing the stresses such that soft switching could still be maintained.

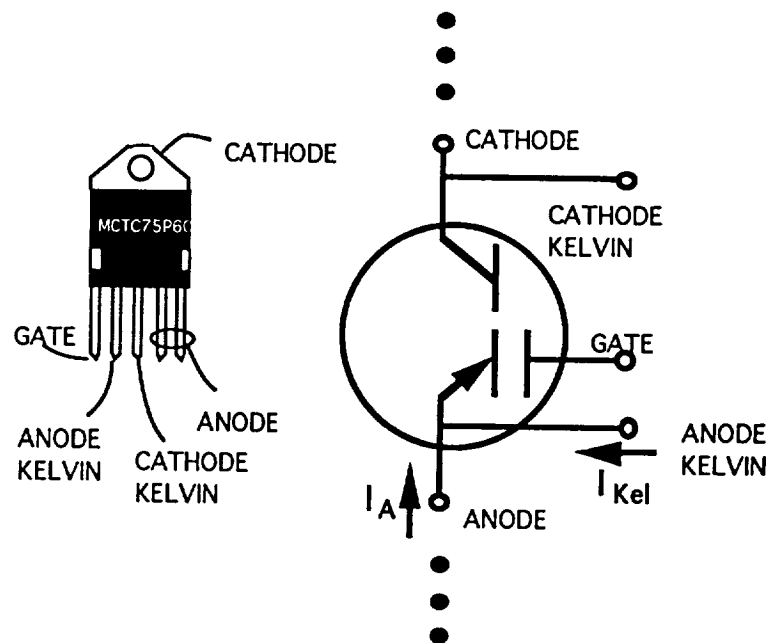


Fig. 4.23 The MCT pin-out and symbol.

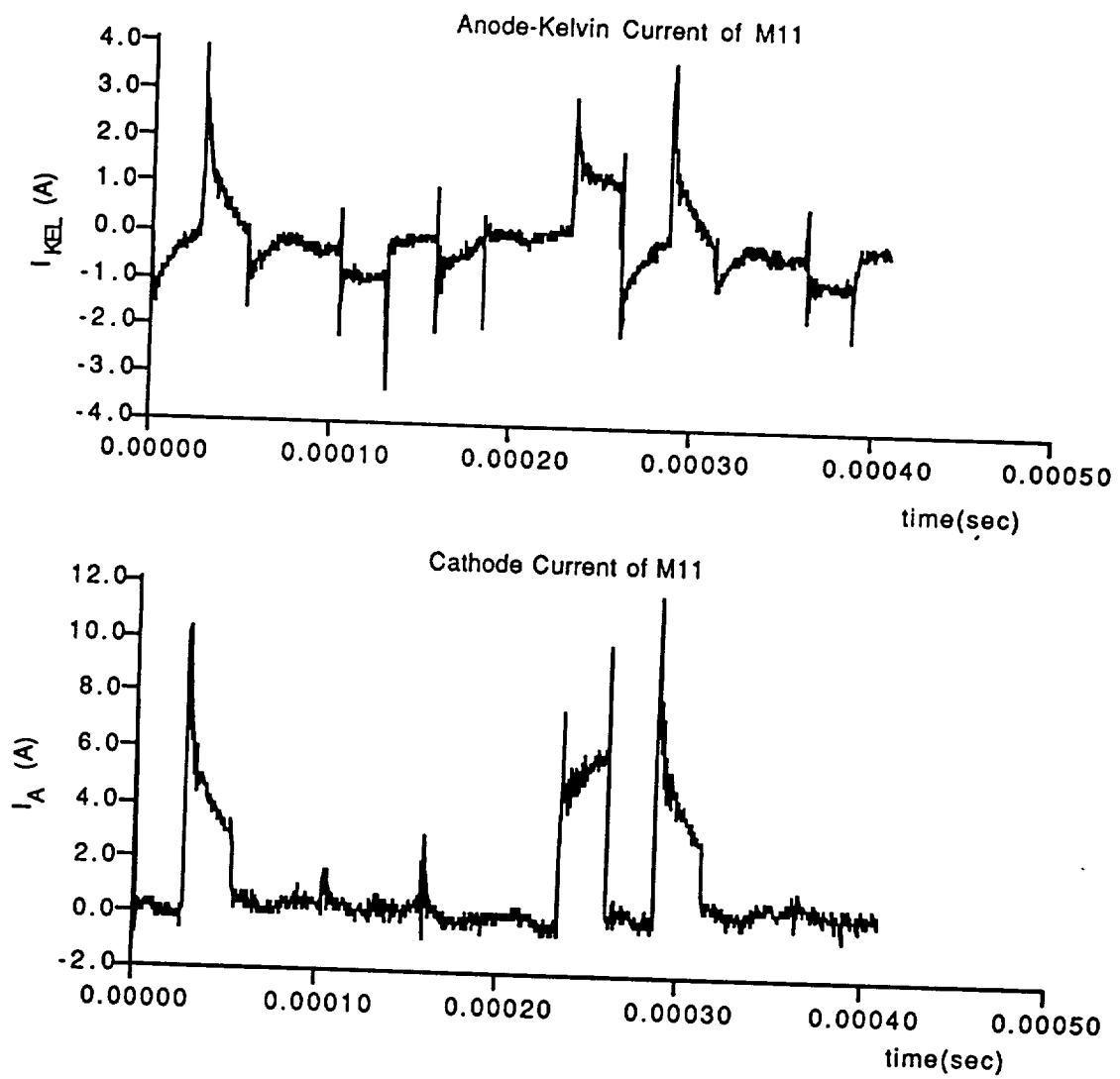


Fig. 4.24 (a) Anode Kelvin Current I_{KEL1} of M1, (b) Cathode current of M11.

CHAPTER V

TESTING THE MCT IN A THREE PHASE CURRENT-REGULATED AC/AC PDM CONVERTER

5.1 Introduction

In an ac/ac PDM converter, low frequency voltage is obtained by switching a high frequency ac link at zero crossing voltages as shown in Fig. 5.1. There are many advantages to switching at zero voltage. For example, switching losses are minimized. Also the switch is not required to support a step in voltage at turn-off, therefore the converter does not need switching devices with as high as of a dv/dt rating as in a hard switched pulse width modulation (PWM) inverter.

PDM converters can be developed using a variety of different topologies. These include single phase converters and three phase converters with ac and dc links. One of the most advantageous configurations for the electromechanical systems is the three phase ac link converter.

5.2 Three Phase Ac Link PDM Converter

Figure 5.1 shows a single phase and a three phase ac/ac PDM (pulse density modulation) converter. Although either an ac link or a dc link can be used to generate a PDM signal, ac has advantages over dc in many aspects such as safety and isolation. A phase voltage can be obtained by switching S_a and $\overline{S_a}$ at zero crossings of the ac link such that a low frequency component voltage is obtained, see Fig. 5.1(a). Note that in the PWM case the four switches are needed to get single phase. In PWM the instantaneous

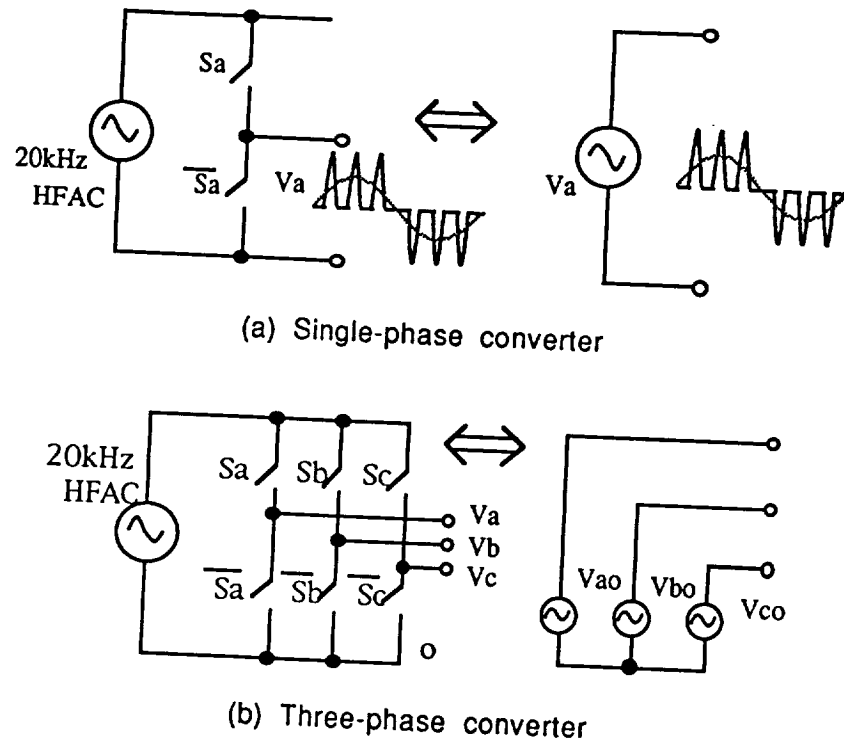


Fig. 5.1. Demonstration of single- and three-phase ac/ac converters.

average voltage is controlled by changing the pulse width. While in PDM the voltage is controlled by changing the number of pulses. The value of each pulse equals the average voltage of a half cycle of the ac link. A three phase PDM converter can be represented by three low frequency voltage sources is shown in Fig. 5.1(b).

Although the PDM converter minimizes switching losses as mentioned above, the device ratings and speed requirements, compared to those of PWM inverters, might constitute some disadvantages of this converter.

Peak voltage requirement: The peak voltage of the ac link is higher than the dc level for a PWM inverter. The pulse value has to be high enough so that it can be modulated to a low frequency voltage with a wide range of amplitudes. Figure 5.2, for example, shows the maximum possible line-to-line voltage of a PDM converter for a given ac source. The line-to-line voltage is maximum when the phase voltages have the

maximum pulse density. It can be seen from Fig. 5.2 that one third of a fundamental cycle has zero voltage and the other two thirds are fullwave rectified. The average of a fullwave rectified voltage is given by

$$\langle V_{FW} \rangle = \frac{2}{\pi} |V_{in}| \quad (5.1)$$

therefore, the average the line-to-line voltage can be approximated by a square wave as shown in Fig. 5.2(b). The maximum possible line-to-line fundamental amplitude can be found by using Fourier analysis. Assuming that high frequency pulses are very small in the limit the line to line voltage magnitude becomes :

$$|V_{LL}| = 2 \cdot \frac{2}{2\pi} \int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} \left(\frac{2}{\pi} |V_{in}| \right) \sin(\omega t) d\omega t$$

$$|V_{LL}| = 0.702 * |V_{in}|$$

$$V_{LL \text{ RMS}} = \frac{0.702}{\sqrt{2}} * |V_{in}| = 0.496 * |V_{in}| \quad (5.2)$$

From (5.2), we can find the maximum fundamental rms voltage for a given high frequency voltage source. For example, to drive a 230V motor, the peak voltage of the ac link needs to be 464V, but only about 300V dc voltage is needed if a PWM inverter is used. The devices used in a PDM converter must, therefore, be able to block higher voltage than used in a PWM converter.

On voltage Drop: Since most the existing fast switching devices do not block high reverse voltage, a series diode is needed when there is reverse voltage like in an ac/ac PDM converter. A bi-directional switch consisting of two switching devices and two diodes is usually used, as shown in Fig. 5.3. When on, the switch can conduct

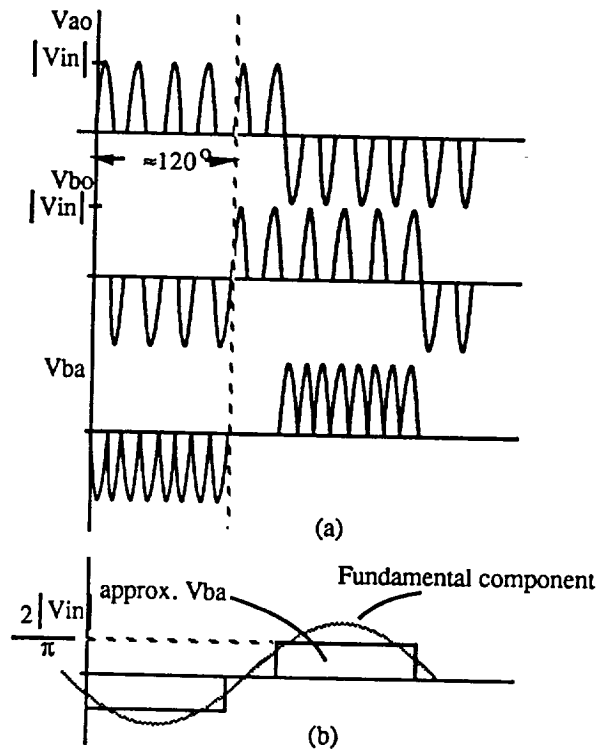


Fig. 5.2 (a) Example of maximum possible fundamental, line-to-common, V_{ao} , and line-to-line voltages, V_{ba} . (b) maximum possible equivalent line-to-line voltage.

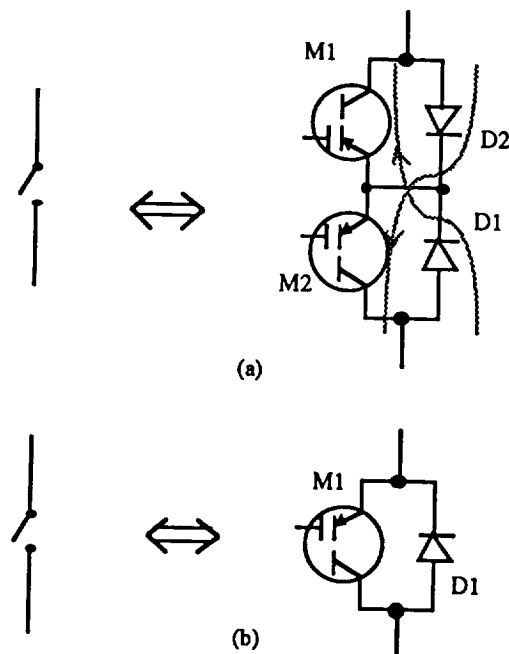


Fig. 5.3 Implementation of a Bidirectional switch for (a) ac link converters (b) dc link inverters

current in both polarities. The on-voltage drop equals to the sum of the on-voltage of a device and a diode and is high when compared to PWM inverters. In a PWM inverter there is only one switch voltage drop as shown from the switch implementation of Fig. 5.3(b). The additional voltage drop in the PDM converter causes high conduction losses. There is no advantage of using a PDM converter if the conduction loss alone is higher than the total losses of other similar converters.

Critical switching timing: The time between two zero crossings of a 20kHz ac source has only 25 μ s. As pointed out in earlier, turn-on of one switch and turn-off of the other in one leg (e.g. S_a and $\overline{S_a}$) of a three phase PDM converter must be completed instantaneously, otherwise an instant of short or open circuit in one leg will happen. With the proposed snubber circuits, a small error of $\approx 1\mu$ s in switching timing is allowed, but the devices are still required to be able to support high di/dt and dv/dt and have fast turn-on and turn-off time.

A general comparison of the features and disadvantages of the PDM converter and a PWM inverter is given in Table 5.1.

An ideal device for ac/ac PDM converter will have high voltage blocking capability, fast switching times and low on-voltage drop. Thus, the disadvantages of the ac/ac PDM converter limit the choices of switching devices. The features of the MCT makes it the most promising candidate for this application.

5.3 Current Regulated Ac/ac PDM Converter

Current regulation is a simple method of implementing feedback control on power converters. The output current is controlled so that it follows the command or reference current.

These disadvantages have to be considered in order to design a better ac/ac PDM converter. To overcome them specific demands on the device ratings must be made.	Three Phase ac/ac PDM Converter	Three Phase PWM Inverter
Voltage Source	High Frequency ac link	DC Link
Peak off Voltage Across each switch	$\approx 2 * V_{LL}$	$\approx 1.4 * V_{LL}$
Critical switching timing	Yes	No
Number of devices	12 switching devices and 12 diodes	6 switching devices and 6 diodes
Soft switching	Yes	No
On voltage Drop of each device	1 switching device and 1 diode	either 1 switching device or diode

TABLE 5.1. A General Comparison Of PDM and PWM Technique

5.3.1 Single-phase current regulation

Figure 5.4 shows the control scheme for a single-phase current regulated ac/ac PDM converter. Since the load current is not fast changing compared to the high

frequency ac link, the error current e_{ia} is sampled only at the rising edges of the zero crossings of the ac source rather than at every zero crossing. When the error current e_{ia} is negative, a positive voltage pulse will force the increase in the output current I_a , and the opposite for positive e_{ia} . An example waveforms of I_a , I_a^* and V_a is demonstrated in Fig. 5.4.

1) Switching frequency: In a similar current regulated PWM inverter, a hysteresis comparator is used so that the switching states will change only when the error current is above some value. Otherwise the switching frequency becomes unboundedly high and might eventually damage the switching devices due to thermal dissipation. In PDM the maximum switching frequency is limited to twice as that of the ac link i.e. about 40kHz. With a two state (positive-negative) comparator, the total number of switchings in a PDM converter is significantly higher than a PWM inverter because it is essentially the number of zero-crossings of the ac source. A PDM

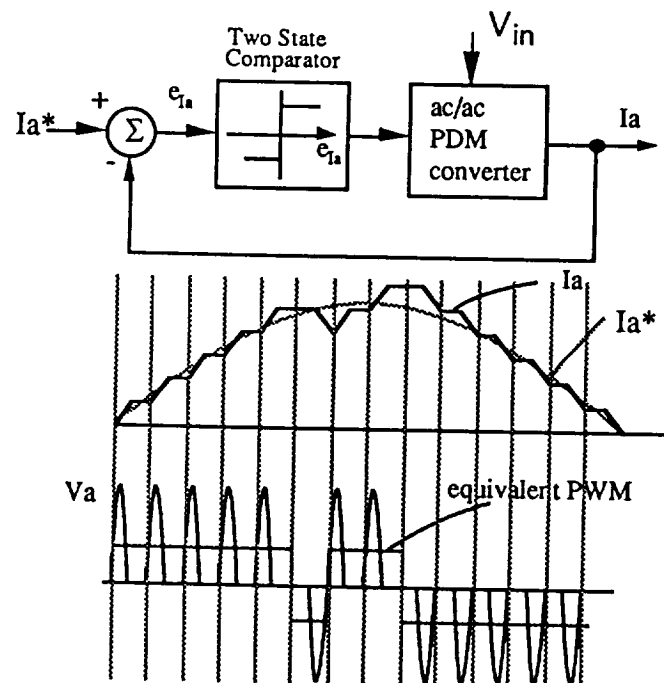


Fig. 5.4 Current regulation of a single phase PDM converter using a two state comparator.

converter with two state switching and an LR load with low frequency back emf (see Fig. 5.6) is simulated and the result is shown in Fig. 5.7. As can be seen from the voltage waveform, the switching states have to change every cycle, the number of switchings is, therefore, 40,000 per second (in fact it is slightly less than that because the switching state remain unchanged when e_{ia} has a positive-to-negative or negative-to-positive transition.)

To minimize the number of switchings, a three state comparator (as shown in Fig. 5.5) can be used. In this case a zero-state describes the error current within a small tolerance. During the zero-state, a switch in one leg remains on for a full ac cycle. The average voltage applied to the load over this cycle is zero and the number of switchings is then zero. The same circuit used for simulating two-state switching is simulated with three state switching and is shown in Fig. 5.8. In this particular example, zero state is considered when the error current is within 3% of the peak

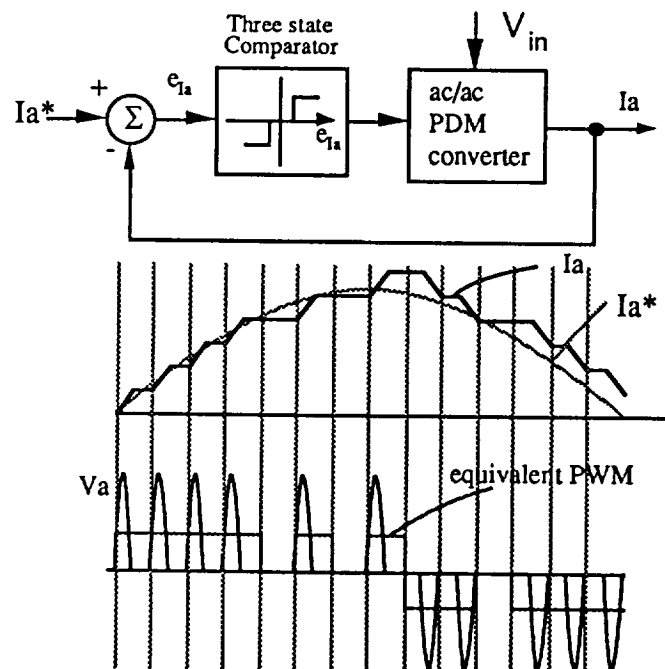


Fig. 5.5 Current regulation of a single phase PDM converter using a three state comparator.

command current. It can be seen that the switching states do not change as often as in Fig. 5.7 and the current has less ripples. In the experimental result, however, the three state comparator is not used.

2) High frequency ac source: A Mapham inverter [10] is used in both of the simulations and experiment. As seen in Figs. 5.7 & 5.8, the ac voltage does not have constant peak value every cycle, this is because the Mapham inverter was not acting like an ideal voltage source. A step change in load current can cause transient voltage in the output of the Mapham inverter.

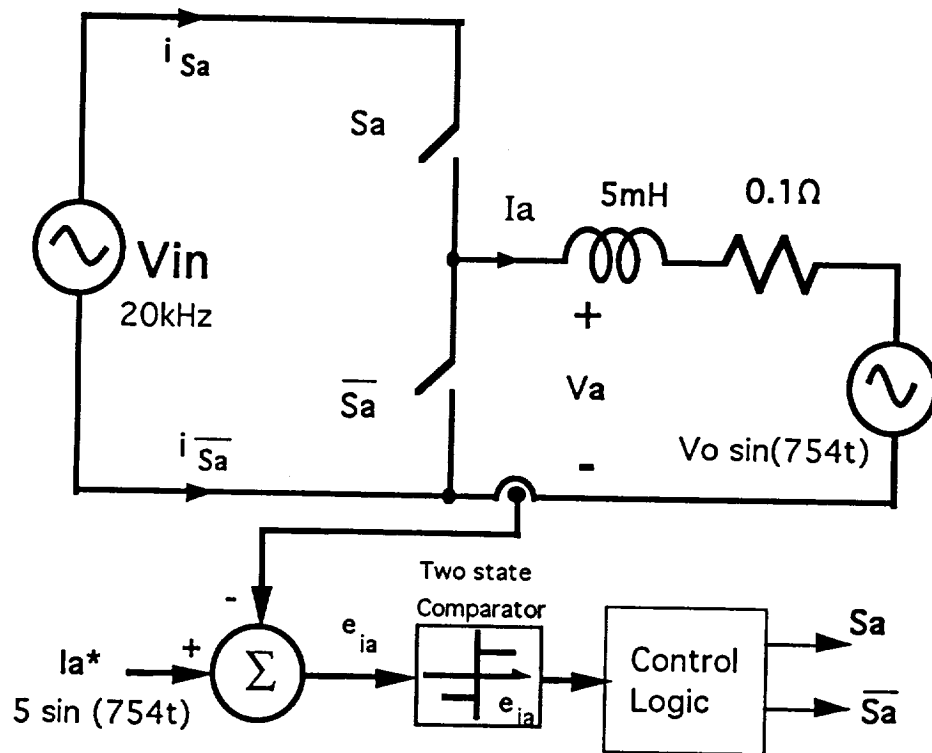


Fig. 5.6 Single-phase current regulated PDM converter to be simulated.

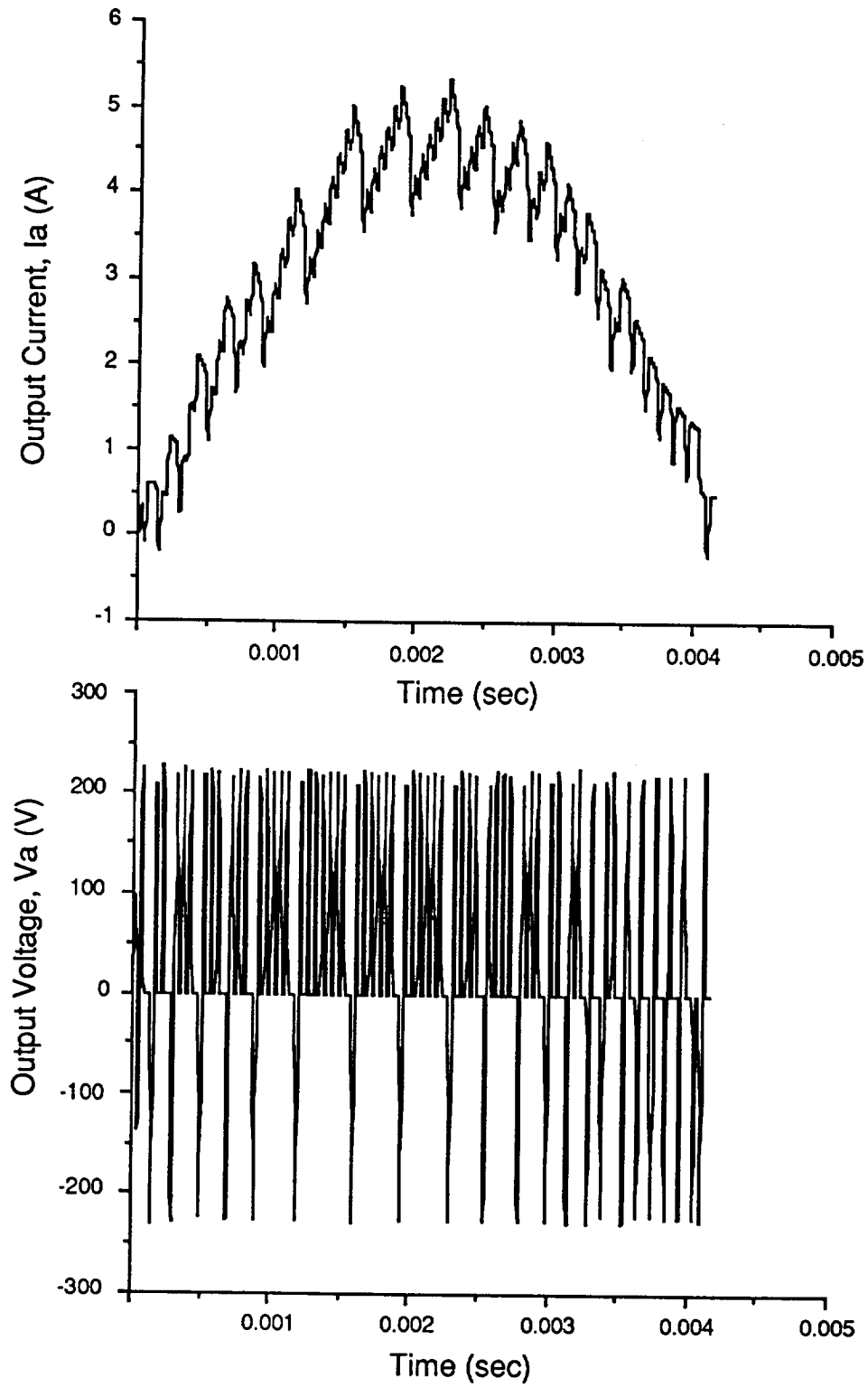


Fig. 5.7 Simulations of Output Voltage and Current using two-state switching.

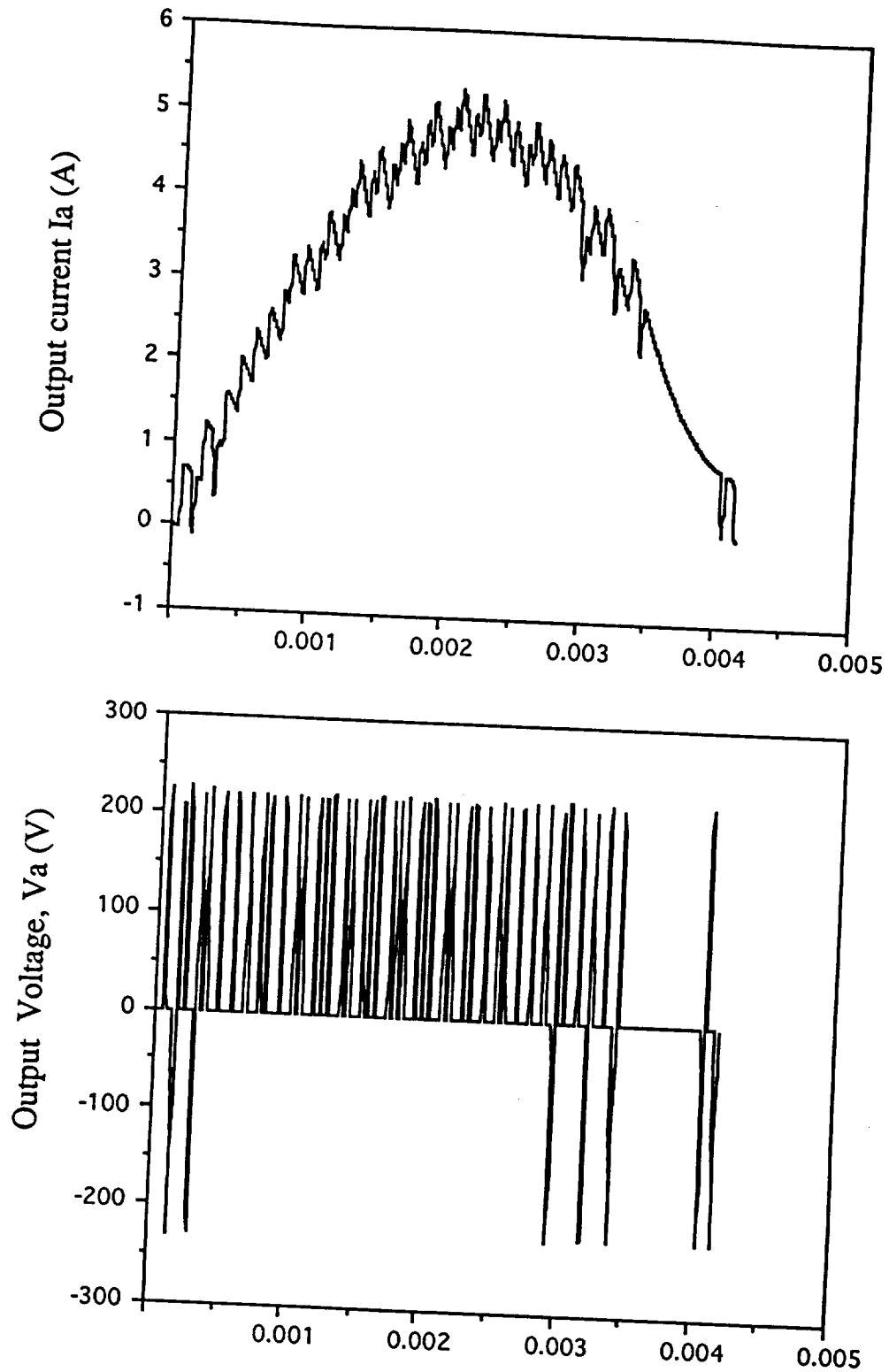


Fig. 5.8 Simulation of Output Current and Voltage using three state switching, zero-state is chosen when error current e_{ia} is within 3% of the peak command current.

5.3.2 Three-phase current regulation

Figure 5.9 shows the circuit of a three-phase ac/ac PDM converter with a simplified block diagram of the controller. By the same principle as in the single phase case, each line current in the three phase ac/ac converter is regulated independently according to the error currents e_{ia} , e_{ib} and e_{ic} . Note that the error current e_{ic} is calculated from e_{ia} and e_{ib} . These error currents are only needed to sample at the rising edges of the zero-crossings of the high frequency ac link.

With current regulation this converter acts like a three phase current source. When used in utility interfacing, the command currents should be in phase with the voltage from the power companies so that it can transmit energy with the maximum power factor.

When used as an induction motor driver, this converter regulates the stator currents. That is, the stator current is directly controlled and follows the command currents. Using plain three phase sinewaves as the command current does not efficiently control, the flux (Φ_m) and output torque (T_e). With current regulation, however, this converter becomes portable and compatible with other control methods such as vector controls. As shown in Equation (5.3), controlling the direct-axis current, i_{ds} , and the quadrature-axis current, i_{qs} , can directly control the flux and torque of the induction motor.

$$T_e = K |\Phi_m| i_{qs} = K' i_{qs} i_{ds} \quad (5.3)$$

The command currents i_a^* and i_b^* can be calculated from the flux or stator current information using Equation (5.4). Therefore i_a^* and i_b^* are considered being controlled by a outer loop.

$$i_a^* = i_{qs}^{s*} \quad (5.4a)$$

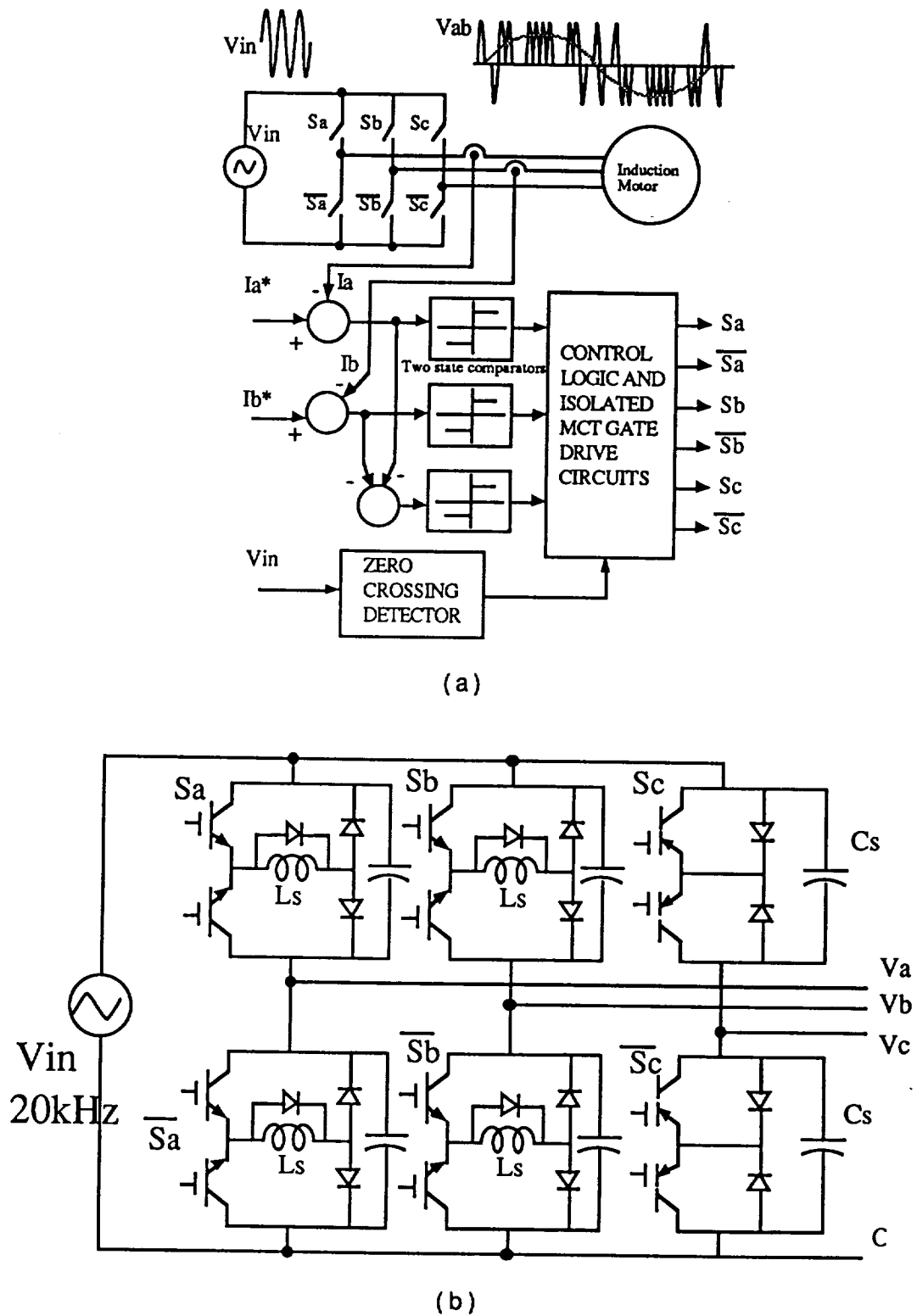


Fig. 5.9 (a) Implementation of a three phase current regulated ac/ac PDM converter.
(b) the three phase PDM bridge

$$i_b^* = -\frac{\sqrt{3}}{2} i_{ds}^* - \frac{1}{2} i_{qs}^* \quad (5.4b)$$

where i_{ds}^* , i_{qs}^* are in the synchronous reference frame.

If speed control is desired, an outer speed control loop will be needed to find the command torque.

5.4 THE DRIVE CIRCUIT

As mentioned in Chapter Three, the MCT needs a gate drive circuit that can provide a rise time of 200ns or less. Six isolated drive circuits need to be used in this experiment. Although a drive circuit using discrete components was designed tested in Chapters Two and Three, a new drive circuit as shown in Fig. 5.10 consisting of ICs is more cost effective and compact especially when six of them are needed. The output voltages are -12V and +16V.

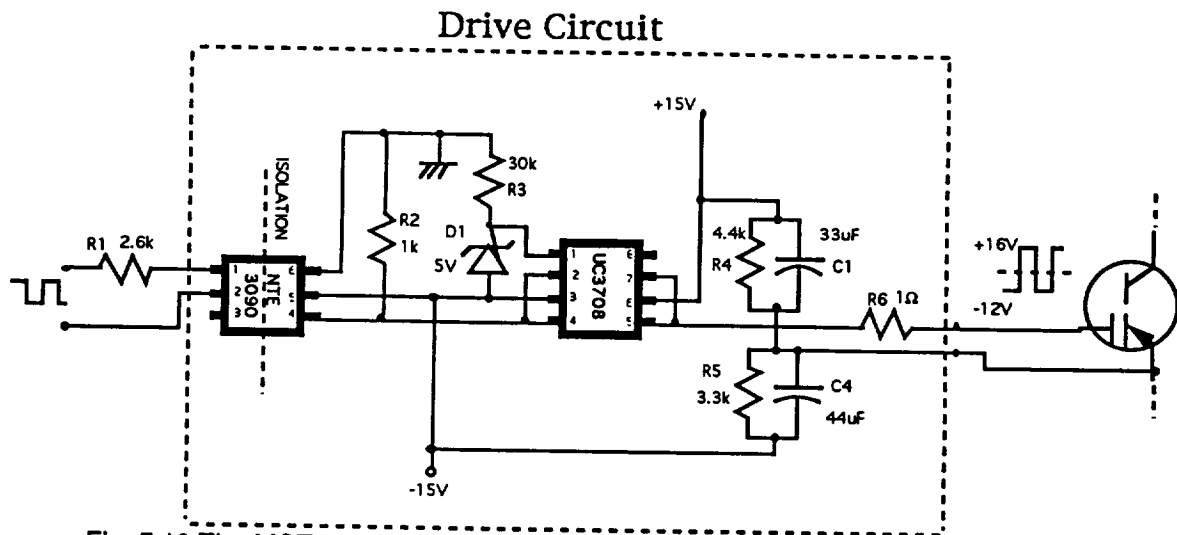


Fig. 5.10 The MCT and IGBT drive circuit used in the ac/ac PDM experiment.

5.5 Experimental Results

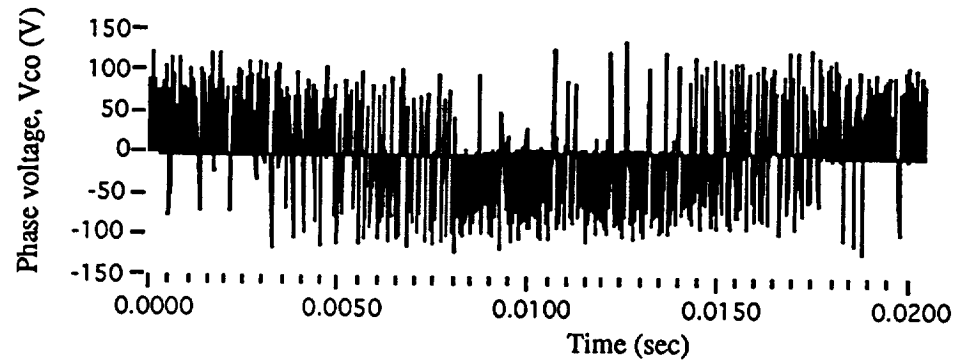
This experiment is set up as the block diagram shown in Fig. 5.9(a), (b). A resonant (Mapham[10]) inverter is used to supply a 20kHz ac source, V_{in} . The

Mapham inverter is not a ideal voltage source, especially when driving a non-linear load like a PDM inverter in which the direction of the current changes so often. Because of this non-ideality during some transients the voltage is not symmetrical about the horizontal axis as will be seen later. Also due to the thyristor rating in the Mapham resonant inverter, the ac link voltage and frequency can only go up to 120V and 15kHz when driving the 5hp induction motor.

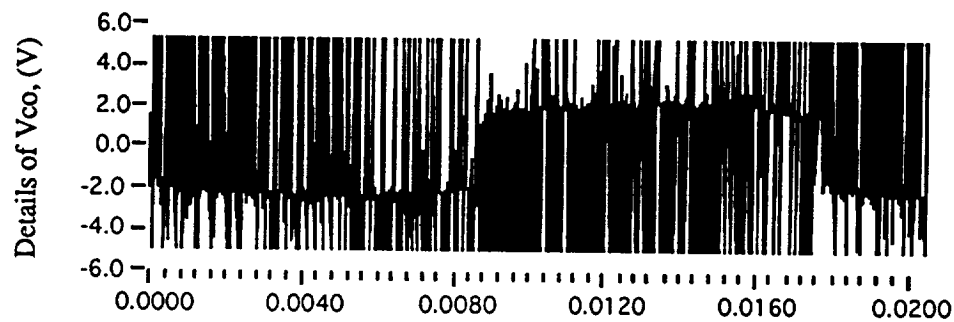
Fig. 5.9(b) shows the three phase PDM bridge with six bi-directional switches. Each switch in phase C consists of MCTs and diodes as shown in Fig. 5.2. However, switches in phase A and B are made of IGBTs and diodes. Each switch is protected by the snubber capacitor, C_s , which keeps the inductive load current continuous in case of an instant of open circuit which would damage the devices. The saturable snubber inductor, L_s , protects the devices from high shoot through current. However only switches made of IGBTs are protected by the snubber inductors because MCTs have "high di/dt rating and good hard-turn-on capability capacitors allow[ing] use of a snubber consisting of a capacitor alone" [9].

Figure 5.11(a) shows the voltage across \overline{Sc} . Although the ac link voltage, V_{in} , is not well regulated due to the non-ideality of the Mapham inverter, with the current feedback control, line current I_c is sinusoidal as shown in Fig.5.11 (c). The stator inductance filtering the high frequency component makes the current ripple very small and be neglected. The reference current I_c^* is not shown and it is not needed because the error current e_{ic} is obtained from e_{ia} and e_{ib} (see Fig. 5.9).

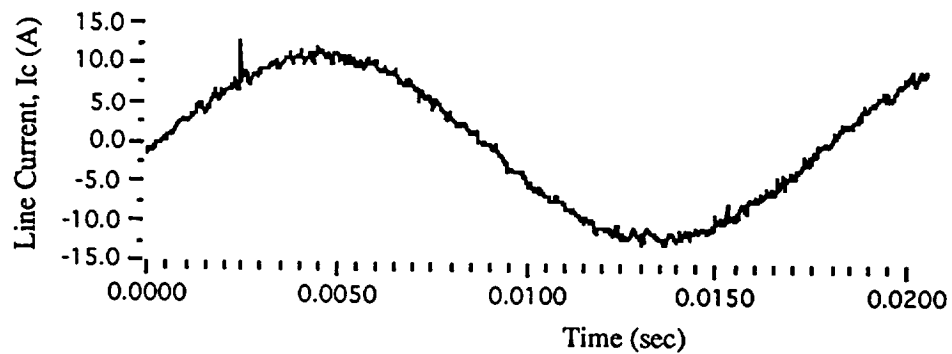
From Fig.5.11(b), an expanded vertical-axis view of Fig.5.11(a). It can be seen that the on-voltage of a bi-directional switch that is made of MCTs is about 2.1V and stays fairly constant for a wide range of the current through it. When compared with MCTs, the switch that made of IGBTs has significantly higher on voltage drop, close to 4V at 11A, which increases with current as shown in Fig. 5.12(a).



(a)



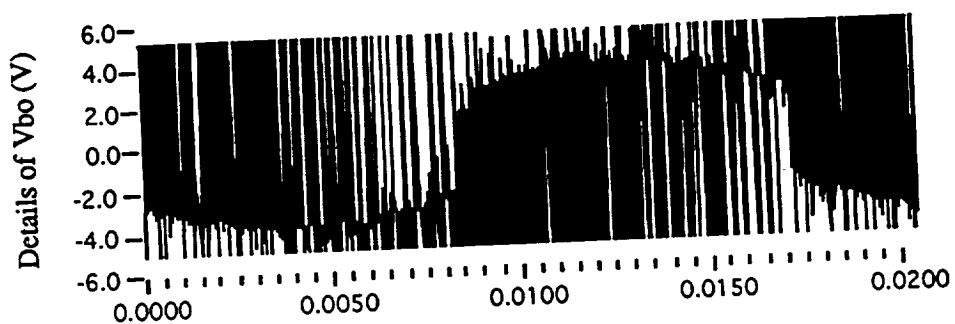
(b)



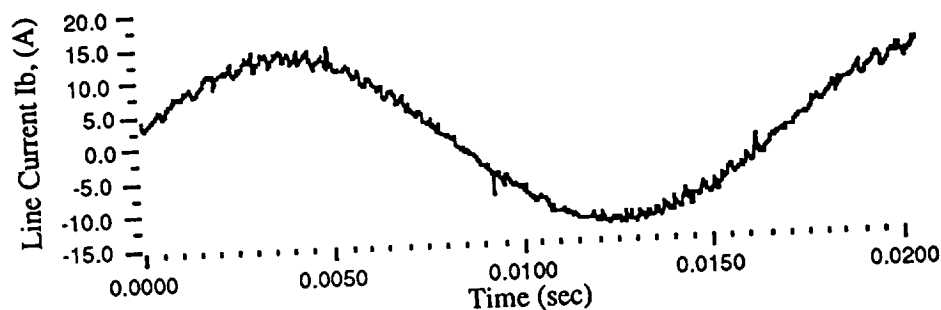
(c)

Fig. 5.11 (a) line-to-common voltage, (b) details of , V_{co} , (C) line current, I_c .

The switching characteristics of an individual MCT are shown in Fig. 5.13 and 5.14. Figure 5.15 (c) shows the instantaneous power dissipated in the MCT and the worst switch loss is found to be $\approx 17\text{mJ}$ during that particular time. The actual on-voltage drop is less than 1.3V at 11A as shown in Fig. 5.14 (a). As explained earlier,



(a)

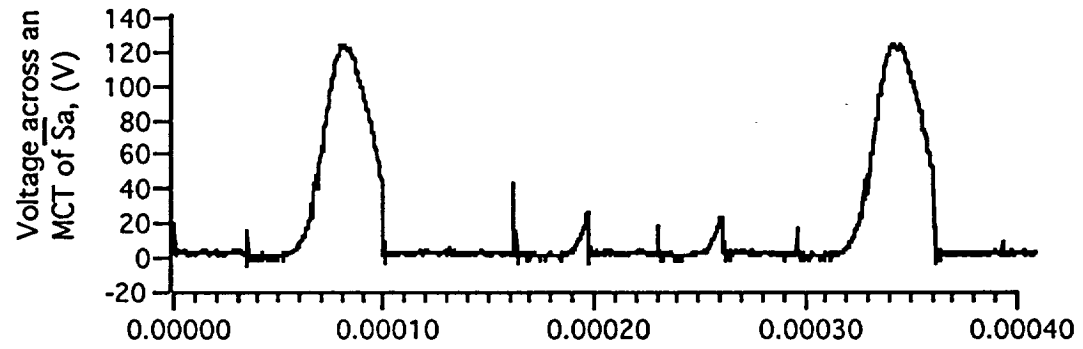


(b)

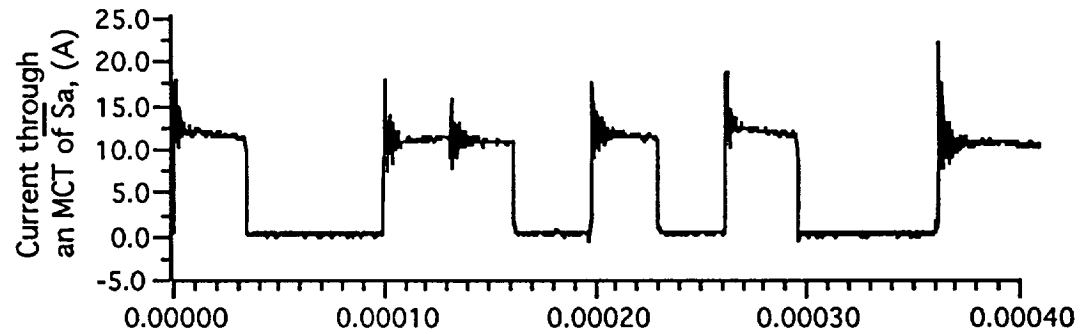
Fig. 5.12 (a)Details of voltage across a switch made of IGBTs, (b)current through the switch.

whenever a bi-directional switch is at zero volts, the individual MCT in the switch is turned on at half of the peak voltage of the ac link. This is because of stored charge in the parasitic capacitors of the anti-parallel diodes. Therefore, in Fig. 5.13 the voltage across the MCT before turn-on is not zero.

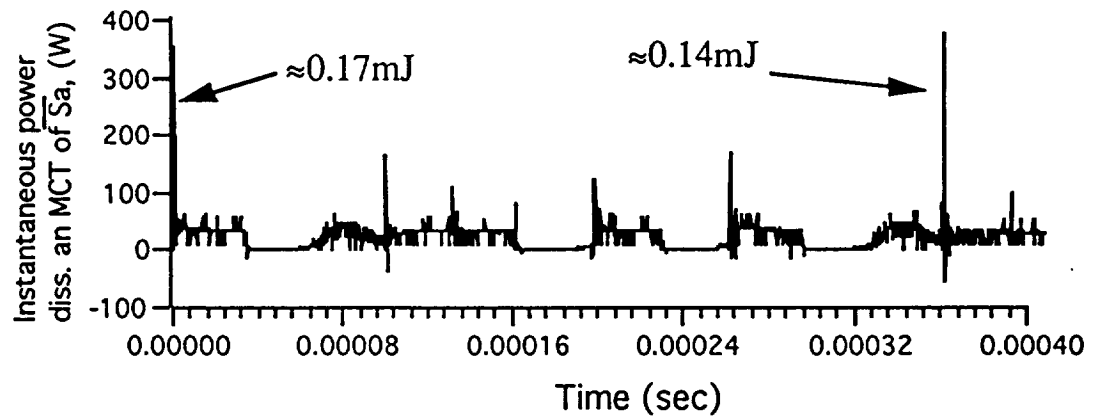
Figures 5.15(a) and (b) show the details of voltage and current of the switch \overline{Sc} . In Fig. 5.15(b), currents steps about 12A each time the MCT is turned on or off. During the particular time shown in Fig. 5.15, the ac link voltage is unsymmetrical about x-axis. Therefore, at some points the switch is turned off a little before or after the zero crossing because the zero-crossing detector was unable to response fast enough to the randomly distorted sinewave. If an ideal ac link was available, this problem would not happen. It can be seen that the switch is able to switch at zero voltage. The switching



(a)

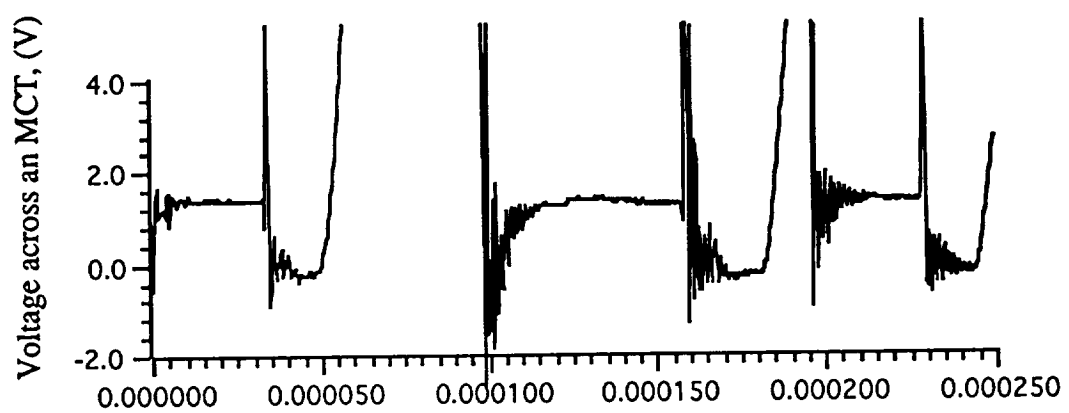


(b)

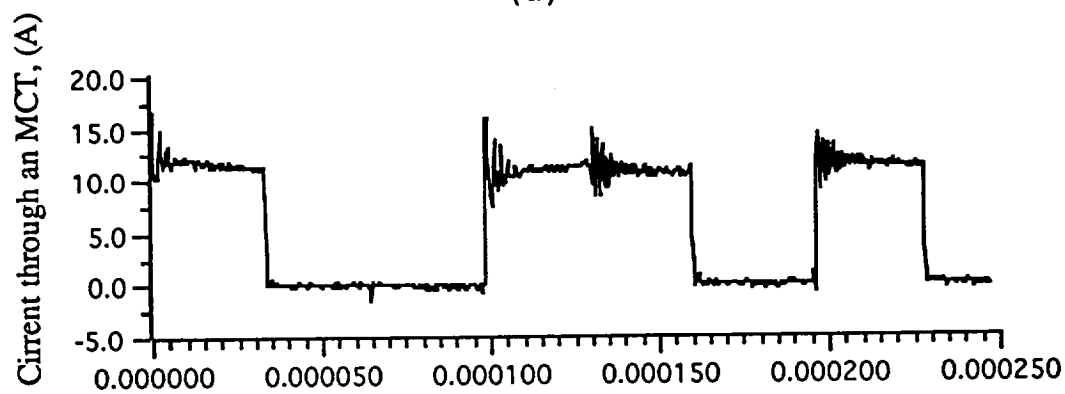


(c)

Fig. 5.13 (a) Voltage across the MCT of a bi-directional switch, (b) collector current through the MCT, (c) product of (a)&(b) (instantaneous power)

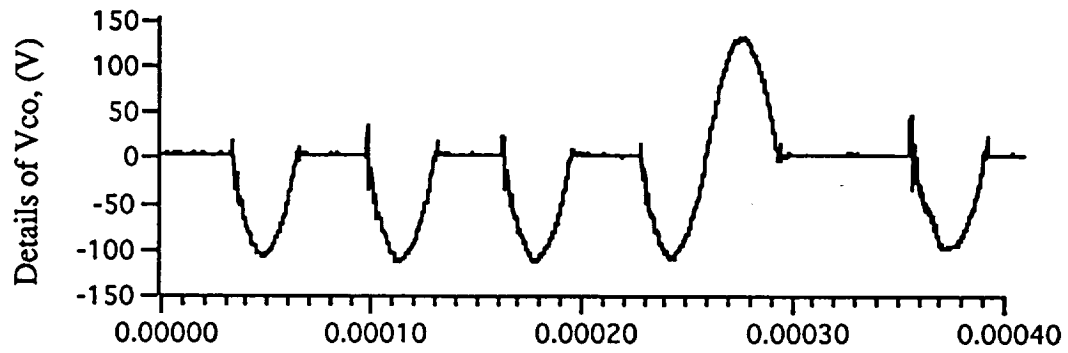


(a)

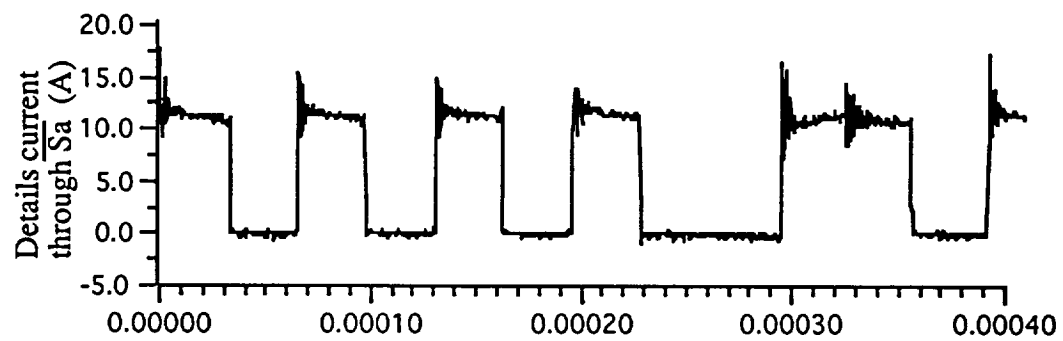


(b)

Fig. 5.14 (a) Details of voltage across an individual MCT, (b) current through the MCT



(a)



(b)

Fig. 5.15 (a)Details of voltage across a switch made of MCTs, (b)current through the switch.

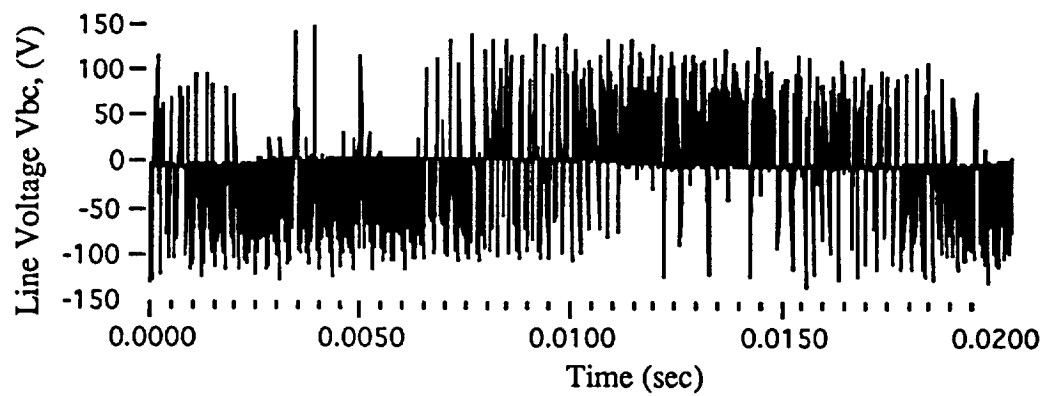


Fig. 5.16 The line-to-line voltage, V_{bc} .

losses are still expected to be small due to the small voltage and short rise and fall time of the current during switching.

Figure 5.16 shows the line-to-line voltage, V_{bc} . It has the same peak value as the phase voltage, V_{co} shown in Fig. 5.10(a), but has a higher density.

Estimated efficiency: The power input to the Mapham inverter can easily be calculated from the dc voltage and current applied. It was found to be about 700W at a standard operation point. The low frequency three-phase output power was found to be about 200W using two-wattmeter method. Therefore the efficiency is about 29%. However, the efficiency of the three ac/ac PDM converter is difficult to measure because the input power from the high frequency ac source cannot be measured with an ordinary wattmeter. It is believed that most power lost in the Mapham inverter due to high resonant current. As the nature of a Mapham inverter, higher load yields higher efficiency (see Appendix 3). The power losses in the PDM converter are estimated in the following.

First, consider the average current through each leg of the converter. This current equals to the peak of the phase current multiplied by $2/\pi$:

$$\begin{aligned} I_{avg} &= I_{peak} \cdot \frac{2}{\pi} \\ &= 13 \cdot \frac{2}{\pi} \\ &= 8.28 \text{ A} \end{aligned} \tag{5.3}$$

One switching in each leg has to be on for any given time. Therefore the conduction loss, P_{cond} , in each leg equals to the on-voltage drop of the bi-directional switch (the diode and the MCT or IGT) multiplied by the average current:

$$P_{\text{cond}} = I_{\text{avg}} * V_{\text{on}} \quad (5.4)$$

The on-voltage of those made of each MCT is $\approx 1.9\text{V}$ (Fig. 5.11(a)), and that of an IGT is $\approx 3.5\text{V}$ (Fig. 5.12(a)). Therefore the total conduction loss of the PDM bridge is

$$\begin{aligned} P_{\text{cond}} &= 8.28 \text{ A} * (1.9 \text{ V} + 3.5 \text{ V} + 3.5 \text{ V}) \\ &\approx 74 \text{ W} \end{aligned}$$

Under accurate zero-crossing switching, the conduction loss is dominant to the switching losses. From 5.14(c) the worst switching loss was 0.17mJ , even it were to happen every time it switches the loss would only be $15\text{kHz} * 0.17\text{mJ} = 2.55\text{W}$, but it should be much smaller and can be ignored. So, the efficiency of the PDM converter can be calculated as:

$$\begin{aligned} \text{eff \%} &= \left(1 - \frac{P_{\text{cond}}}{P_{\text{cond}} + P_o} \right) * 100\% \\ &\approx 73\% \end{aligned}$$

This is, however, a little higher than the actual efficiency because there are always switching losses in the PDM converter due to not switching at zero voltage.

In conclusion, the MCTs connected in a bi-directional switch configuration performed satisfactorily in an ac/ac PDM converter. It is especially better than other devices when used in applications that require critical timing and high voltage blocking capability. The output current of the PDM converter is well regulated by the current feedback scheme presented in this Chapter. Incorporation of this converter with some other control methods will be considered as future work.

For this ac/ac PDM to be tested with full power, a well regulated 20kHz voltage source is needed. As an attempt to run this ac/ac PDM converter at high power,

the 10kW Mapham Inverter from NASA Lewis Research Center was used. Unlike the converter at the University of Akron the voltage of this Mapham inverter could not be increased gradually causing a high $\frac{dv}{dt}$ across the device when the converter was connected to the ac link. The controller was not able to respond safely to the transition causing a few MCTs to be damaged during start-up. The circuit was then modified to the circuit shown in Fig. 5.17. The switch 'PW' was placed before the LC tank so that the $\frac{dv}{dt}$ across the bridge was limited. To ensure the clock signal 'clk' is stable, the switch 'EN' was not opened until the ac link voltage was stable. In other words, the gating signals remained unchanged until 'EN' is opened. The starting sequence is turn on 'PW' first then 'EN'.

More MCTs were damaged as the voltage on the ac link was increased. It was suspected that this damage was caused by a loose connection between a control signal and a drive circuit. Unfortunately, these failures depleted the supply of MCTs, and, therefore, it was not possible to run the converter at full power.

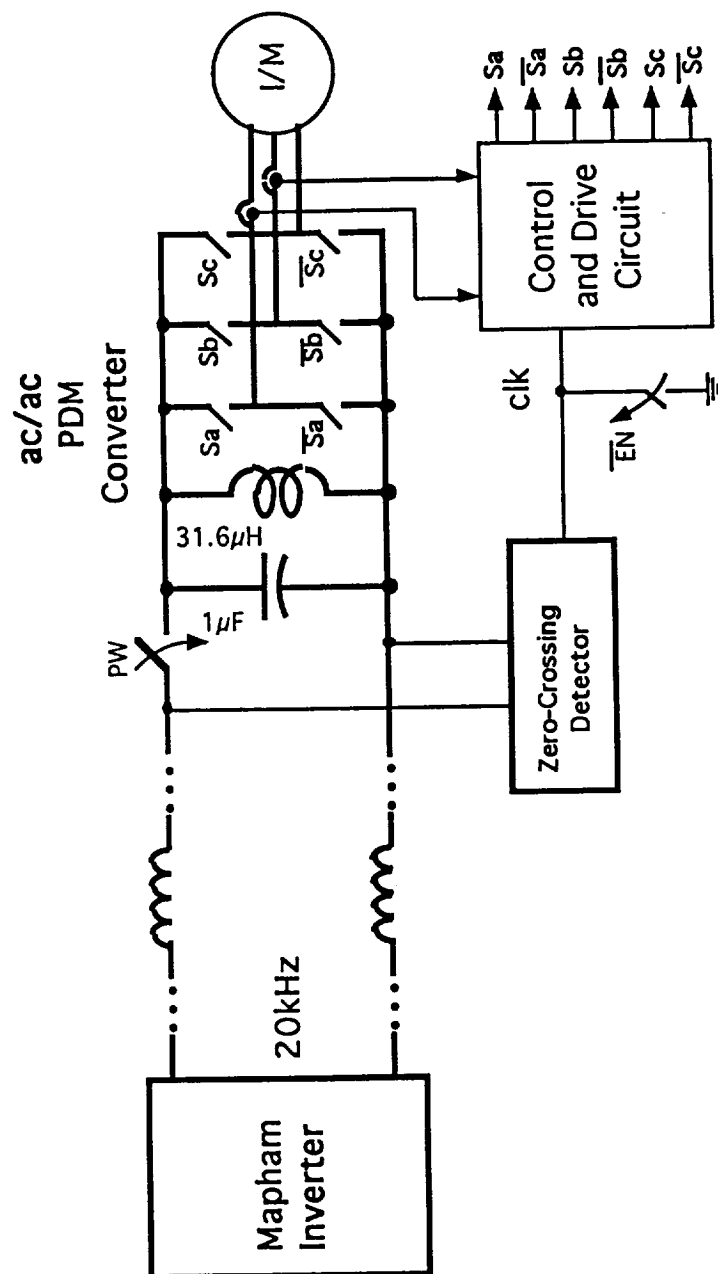


Fig. 5.17 The ac/ac PDM converter with a modified starting sequence.

CHAPTER VI

SUMMARY AND SUGGESTED FUTURE WORK

6.1 Summary

As semiconductor technology rapidly progresses, the speed and power density of many devices have enabled many power electronics systems to operate at higher frequencies and power. The advantages of using high frequency ac power distribution in space application has been studied. Other than making high voltage more safe, reducing component sizes and weights and easily providing isolation, the high frequency ac link can also be used as a voltage source for ac/ac pulse-density-modulation (PDM) converters.

An ac/ac PDM converter directly modulates the high frequency ac source to a several orders of magnitude lower frequency such as 60Hz. The 20kHz component is usually filtered by the load like an induction motor. The major advantage of using a PDM converter is the zero-crossing switching topology which minimizes the switching losses.

The ac/ac PDM converter requires high speed switches that has bi-directional current conduction and voltage blocking capabilities. The configuration of a bi-directional switch is discussed in Chapter Two. For the best performance of the ac/ac PDM converter needs switching device that has low on-voltage drop and fast switching. Among the existing power devices, a MOS-Controlled-Thyristor (MCT) was found to be the best candidates for this application. The MCT is a newly emerged power device which has the best features of a MOSFET and a thyristor.

An initial test was made at 600V/60A MCTs under hard switching. In spite of the MCTs having such a high power handling capability the MCTs have, failures at low voltage and current were experienced. It was noticed in order for the device to operate safely, the the gate drive has to have a fast rise-time of about 200us at turn-off. A discrete gate-drive circuit for MCTs was developed and used for most of the experiments in this research.

In the dc chopper experiment in Chapter Three, the MCT was switched at about 100V and 20A at 20kHz, the devices performed satisfactorily without needing a snubber circuit. Turn-off time is about 1us at 20A and which constitute a major loss in the hard switching experiment. At 30kHz the MCT's turn-off loss increased and caused temperature to rise which further increased the current fall-time, thus thermal runaway occurred. With a turn-off snubber the problem was avoided.

After the hard switching experiment, the device was tested under zero-crossing switching in a single phase ac/ac PDM converter. In Chapters Two and Three and the MCTs were shown to be able to switch at zero volts easily while connected in a bi-directional switch configuration. Although zero-crossing switching topology minimizes switching losses, it was noticed that a difference in turn-on and turn-off delay may harm the devices due to the voltage and current spikes. In practice, completing turn-on of one switch and turn-off of the other at the same moment is difficult to achieve. A bi-directional snubber circuit was designed to protect the device against voltage and current spikes caused by the turn-on and turn-off delays. The snubber circuit limits the magnitude of voltage and current spikes and dissipates the energy that would otherwise be dissipated by the MCTs.

Chapter Five presents the experimental results of a current-regulated three-phase ac/ac PDM converter made of IGBTs and MCTs. One leg of the PDM converter used MCTs and the other two used IGBTs. MCTs and IGBTs have similar characteristics but the

overall features of an MCT such as low on-voltage are better. In the experiment, it was found that the conduction loss of a bi-directional switch made of MCTs is significantly lower than one made of IGBTs. The output currents of the PDM converter are well regulated by the current feedback scheme.

The ac converter was built using 600V/75A MCTs and 600V/25A IGBTs. The converter is designed and is expected to drive a 5hp induction motor at full load. However, due to a latching problem in the Mapham inverter at high load, the converter was not operated at the motor full power level. The thyristors used in the the Mapham inverter have a turn-off time of $15\mu\text{s}$ which is marginal when the inverter is switched at 20kHz. Although, the resonant frequency of the inverter has been reduced to 15kHz so that it allows more time for the thyristors to regain the blocking capability, they still latch as the temperature increases. Under this circumstance, the ac/ac PDM converter has not been tested under full load.

6.2 Suggested Future Work

Being rated at such a high power level, this converter should be tested with higher power such as 5hp.

To made the converter more practical as an induction motor drive, the command currents of the induction motor can be calculated from the flux, torque or speed information. Applying control methods to this converter is considered as future work.

BIBLIOGRAPHY

- [1] Irving G. Hansen, Gale R. Sundberg, "Space Station 20-kHz Power Management and distribution System" Power Electronics Specialists Conference (1986).
- [2] A. C. Hoffman, I. G. Hansen, R. F. Beach, et. al., "Advanced secondary power system for transport aircraft", NASA Technical Paper 2463 (1985)
- [3] K.H.Liu, F.C.Lee. "Zero Voltage Switching Technique in Dc/Dc Converters" IEEE Power Electronics Specialists Conference (1986): 58-70.
- [4] D.W.Novotny, R.D.Lorenz. "Introduction to Field Orientation and High Performance AC Drives" IEEE Industrial Industry Applications Society Annual Meeting (1985).
- [5] R.W. De Doncker, T.M. Jahns, A.V. Radun, V.A.K. Temple, D.L. Watrous. "Characteristics of MOS-Controlled-Thyristors Under Zero Voltage Soft-switching Conditions" Proceedings of the IEEE Industry Applications Society. (Oct. 1989) 1-6
- [6] John G. Kassakian, Martin. F. Schlecht, George. C. Verghese. "Principle Of Power Electronics." Addison-Wesley Publishing Company (1991).
- [7] T.A.Lipo, I.Alan. "System, Component Design and Test of a 10 Hp, 18,000 RPM ac Dynamometer Utilizing a High Frequency ac Voltage Link" NASA Contractor Report, Contract No. NAG3-940 (June 1991)
- [8] Tony Lee, Don S.Zinger, Malik E.Elbuluk. "Modeling, Simulation And Testing Of MCT Under Zero Voltage Resonant Switching" IEEE Industrial Electronics Society Conference (1991): 342-346.
- [9] V.Temple, D.Watous, S.Arthur and P.Kendle. "MOS-Controlled Thyristor(MCT) Power Switches - Part I: MCT Basics" PCIM(November 1992): 9-16.
- [10] N.Mapham. "An SCR Inverter with Good Regulation and Sine-Wave Output", IEEE Transaction on Ind. Gen. Application, Vol. IGA-3, (Mar/Apr. 1967): 176-187.

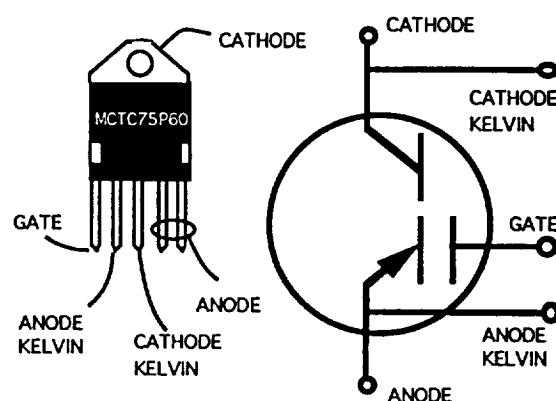
APPENDICES

APPENDIX I

MCT DATA SHEET

P-CHANNEL MOS CONTROLLED THYRISTOR (MCT), MCTA75P60.

- Features:
- MOS Insulated Gate Input
 - Gate Turn-Off Capability
 - 1000 Amp Current Capability
 - 120 Amp turn-Off Capability
 - $V_{tm} = 1.3$ @ $I = 75$ A



MAXIMUM RATINGS, Absolute-Maximum Values ($T_c = 25^\circ\text{C}$)

Peak Off-State Voltage	V_{DRM}	-600	V
Peak Reverse Voltage	V_{RRM}	+10	V
Cathode Current Continuous @ $T_c = 25^\circ\text{C}$	I_{C25}	120	A
@ $T_c = 90^\circ\text{C}$	I_{C90}	75	A
Non-repetitive Peak Cathode Current	I_{TSM}	1000	A
Peak Controllable Current	I_{TC}	120	A
Gate-Anode Voltage Continuous	V_{GA}	± 20	V
Rate of Change of Voltage ($V_{ga} = +15$)	dV/dT	10000	V/us
Rate of Change of Current ($V_{ga} = -10V$)	dI/dT	1000	A/us
Power Dissipation Total @ $T_c = 25^\circ\text{C}$	P_T	208	W

Power Dissipation Derating $T_c > 25^\circ\text{C}$		1.67	W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$
Maximum Lead Temperature for Soldering	T_L	260	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS,

At Case Temperature (T_C) = 25°C unless otherwise specified.

CHARACTERISTICS	SYMBOL	TEST CONDITIONS The test circuit in Fig. A1.1.	LIMITS			UNIT
			MIN	TYP	MAX	
Peak Off-State Blocking Current	I_{DRM}	$V_{AK} = -600\text{V},$ $V_{GA} = +15\text{V}$	$T_C = 150^\circ\text{C}$ $T_C = 25^\circ\text{C}$	- - -	3 100	mA μA
Peak Reverse Blocking Current	I_{RRM}	$V_{AK} = +5\text{V},$ $V_{GA} = +15\text{V}$	$T_C = 150^\circ\text{C}$ $T_C = 25^\circ\text{C}$	- - -	4 100	mA μA
On-State Voltage	V_{TM}	$I_C = I_{C90},$	$T_C = 150^\circ\text{C}$ $T_C = 25^\circ\text{C}$	- - -	1.3 1.4	V
Gate-Anode Leakage Current	I_{GAS}	$V_{GA} = \pm 20\text{V}$	- - -		200	nA
Input Capacitance	C_{is}	$V_{AK} = -20\text{V}$ $T_J = 25^\circ\text{C}$	- - -	- - -	11	nF
Output Capacitance	C_{oss}	$V_{GA} = +15\text{V}$			TBD	nF
Current Turn-on Delay Time	$t_{d(on)i}$	$L = 50\mu\text{H},$ $I_C = I_{C90}$	- - -	- - -	400	ns
Current Rise Time	t_{ri}	$R_g = 1\Omega, V_{GA} = +15\text{V}, -10\text{V}$	- - -	- - -	500	ns
Minimum Rise Time	$t_{(ot)}$		TBD	- - -	- - -	μs
Current Turn-off Delay Time	$t_{d(off)i}$	$T_J = 125^\circ\text{C}$	- - -	- - -	700	ns
Current Fall time	t_{fi}	$V_{AK} = -300\text{V}$	- - -	- - -	1.4	μs
Turn-off Energy	E_{off}		- - -	- - -	15	mJ
Thermal Resistance	$R_{\theta JC}$		- - -	.5	.6	$^\circ\text{C/W}$

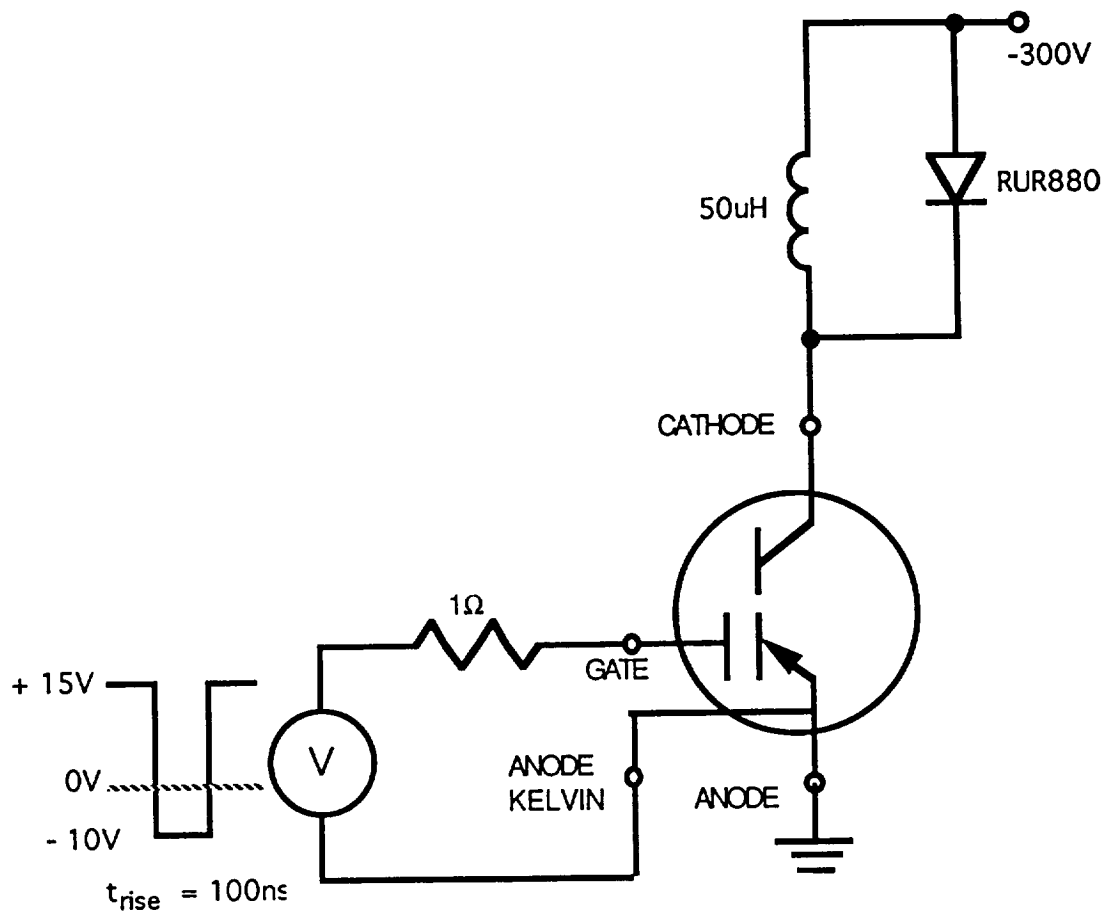


Fig. A1.1 Manufacturer's Test circuit for MCTA75P60.

Handling Precautions for MCTs

MOS Controlled Thyristors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. MCTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as **ECCOSORB LD26** or equivalent.
 2. When devices are removed by hand from their carriers, the hand being used should be grounded by and suitable means - for example, with a metallic wristband.
 3. Tips of soldering irons should be grounded.
 4. Devices should never be inserted into or removed from circuits with power on.
 5. Gate Voltage Rating - Never exceed the gate-voltage rating of V_{GA} . Exceeding the rated V_{GA} can result in permanent damage to the oxide layer in the gate region.
 6. Gate Termination - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage current or pickup.
 7. Gate Protection - These devices do not have an internal monolithic zener diode from gate to emitter. If gate protection is required, an external zener is recommended.
- * Trademark Emerson and Cumming, Inc.

APPENDIX II

THE SCHEMATICS OF THE PDM CONTROL CIRCUIT

The appendix is for the documentation of the three phase ac/ac controller.

Figure A2.1 is the controller that provides the switching state. In this circuit if current limit signal, LMT, is high this circuit will shut off the PDM converter by opening the top three switches S1, S2 and S3 and close the lower three switches. With the jumper "Jump 1" open this circuit functions as a current regulated controller that shown in Fig. 5.8(a). With "Jump 1" closed, the current feedback is disabled and the command currents becomes command voltages to be modulated by the triangle wave "TRI". The frequency of "TRI" is 1/16 of the ac link frequency. The circuit for the "TRI" signal is shown in Fig. A2.2.

Figure A2.3 shows the circuit that generates LMT which is high when the magnitude of the current flowing in to the converter is over the preset current level.

Figure A2.4 is the pinout for interfacing between the converter and the control circuit. The interface connector is a 14 pin dip connector.

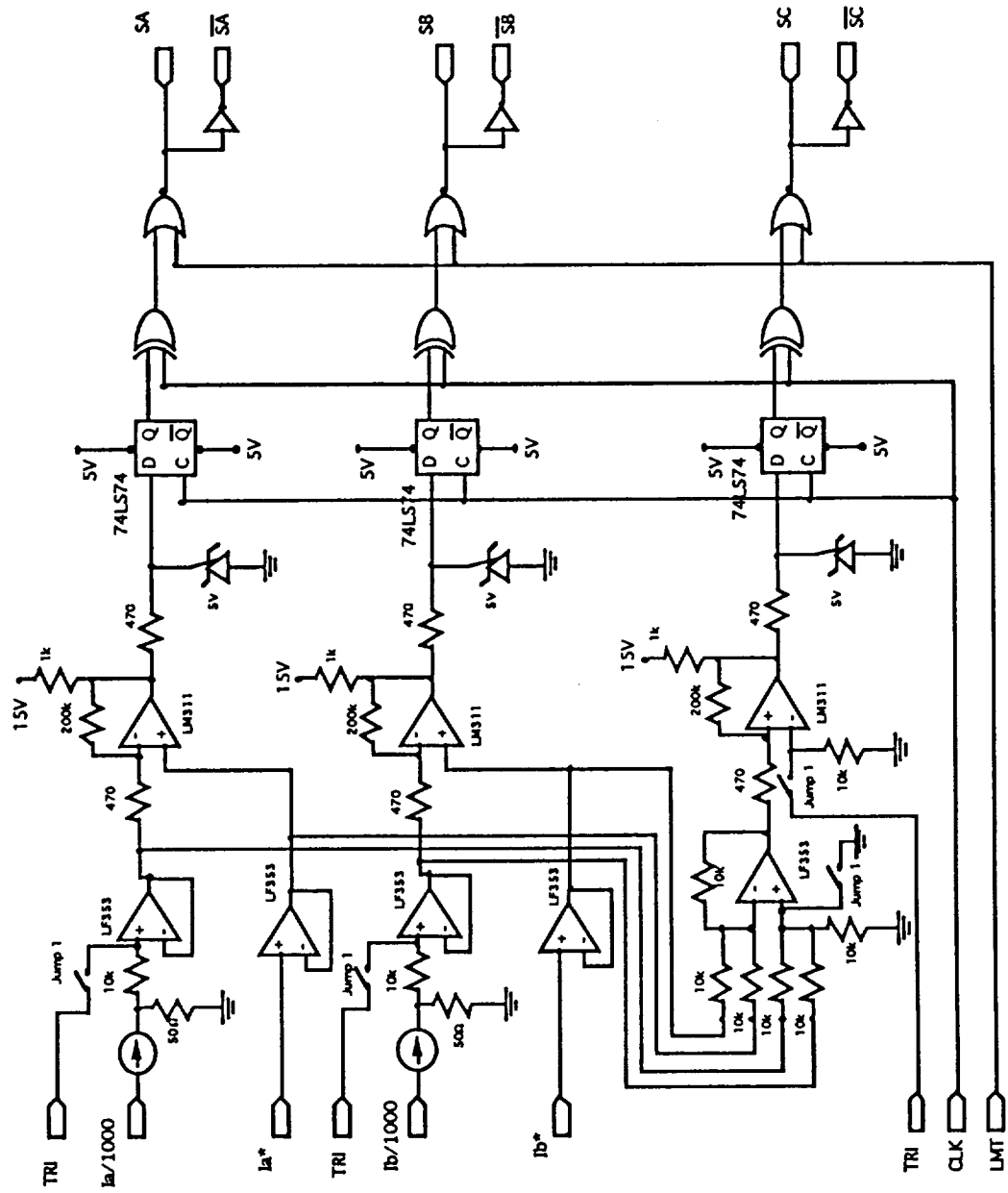


Fig. A2.1 Zero-crossing switching control circuit.

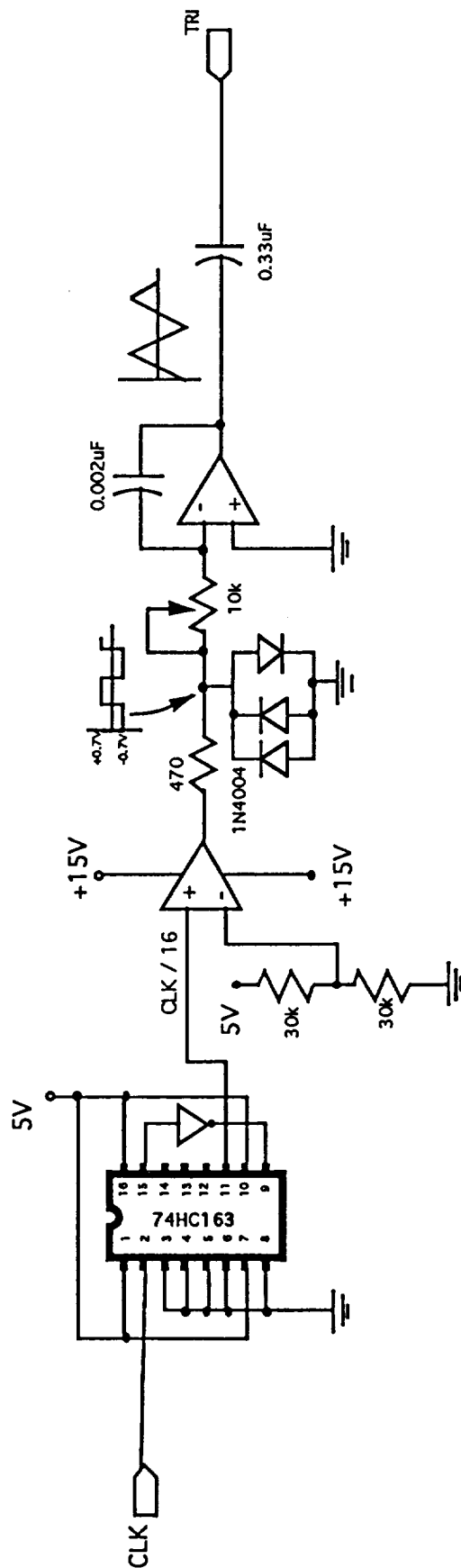


Fig. A2.2 The triangle wave generator that provides "TRI".

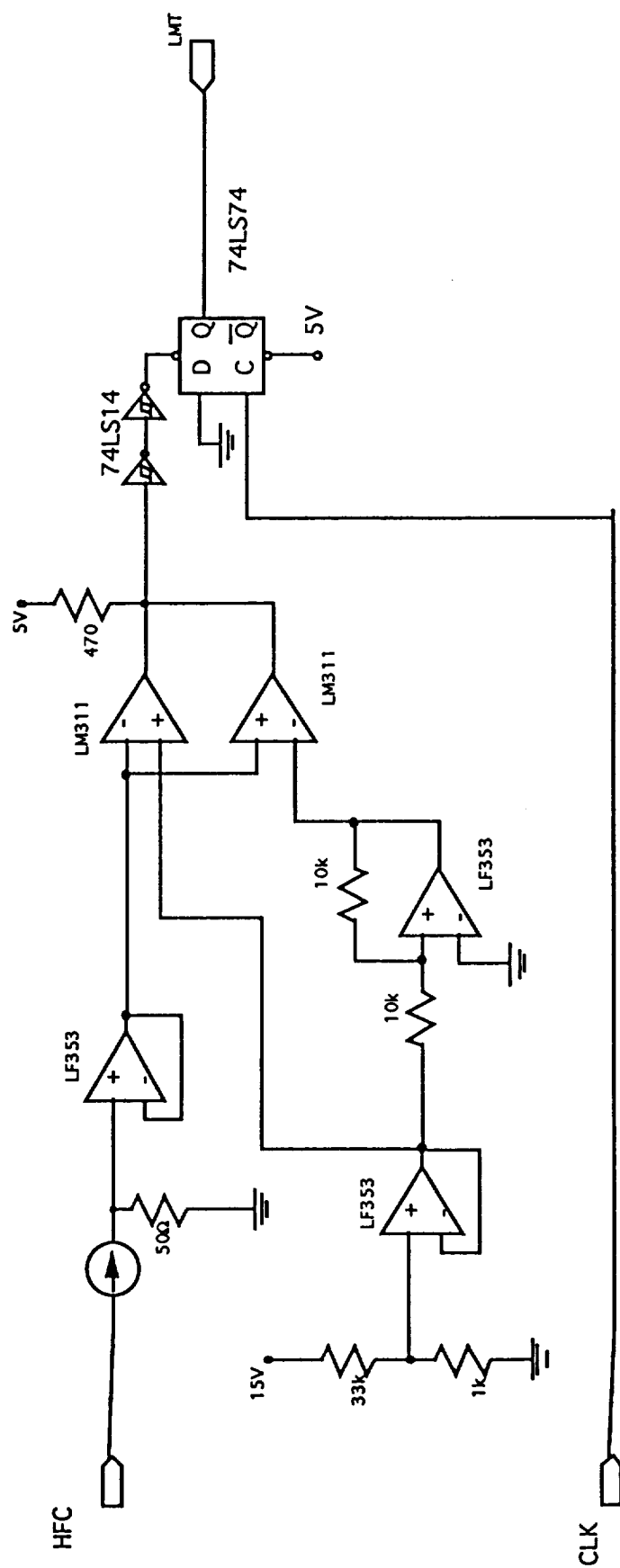


Fig. A2.3 Current limit signal, LMT, generator.

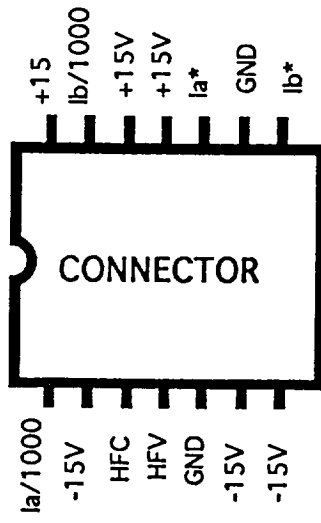


Fig. A2.4 Cable pinout.

APPENDIX III

ANALYSIS AND SIMULATION OF THE 20KHZ AC SOURCE THE MAPHAM INVERTER

Introduction

Traditional ac sources are obtained from synchronous generators, as shown in Fig. A3.1. The magnitude and frequency of the output voltage, V_o are controlled by adjusting the magnetizing field current, I_f , and shaft speed, ω , respectively, of the generator. The advantage of using a synchronous generator is that the output voltage is almost independent of the load, i.e. it is close to an ideal source. However it involves mechanical to electrical power conversions which causes significant of energy losses. As the machines are basically made of iron and copper, they are always bulky and heavy. The prime movers, like a turbine or dc motor, are also very heavy. If high frequency voltage outputs are wanted, a machine would require hundreds of poles that makes the itself even bigger. Such a system is impractical in many applications where space is limited.

In the era of power electronics, a resonant inverter can be used to generate ac in a more convenient way. A dc/ac inverter is made using semiconductor devices, inductors and capacitors. Compared to a synchronous generator, a dc/ac inverter is order-of-magnitude better in terms of cost effectiveness, portability, controllability, power density and efficiency. There are different kinds of resonant inverters, but the principles of how they are operated are the same. The fundamental frequency of the output voltage of a resonant inverter is the same as the switching frequency provided by

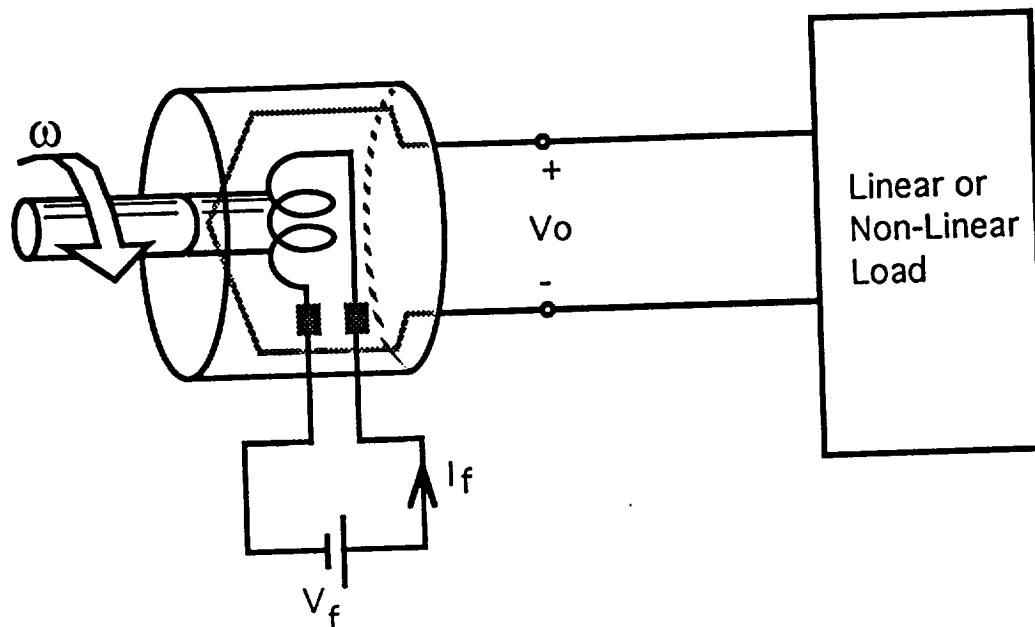


Fig. A3.1 Using a synchronous generator to generate ac voltage.

the control circuit. In most resonant inverters, fully controlled switching devices, like BJTs, MOSFETs etc., are switched so that a square voltage of current is applied to a series or parallel resonant LC circuit. The switching frequency is close to the resonant frequency of the LC circuit which filters the harmonics. The distortion and magnitude of the output voltage of a resonant converter is dependent on the load. For example, a heavy load, which decreases the quality, Q , of the resonant tank, thus causing more harmonic distortion and attenuating the magnitude.

A Mapham inverter[10], as shown in Fig. A3.2, is an improved resonant inverter which is designed to have a better voltage regulation and less harmonic distortion. Another advantage (disadvantage in some cases) of using such a inverter is that thyristors can be used as the switching devices meaning higher power density and easier to drive. Detailed features and analysis of this inverter can be found in [10] and the related literatures.

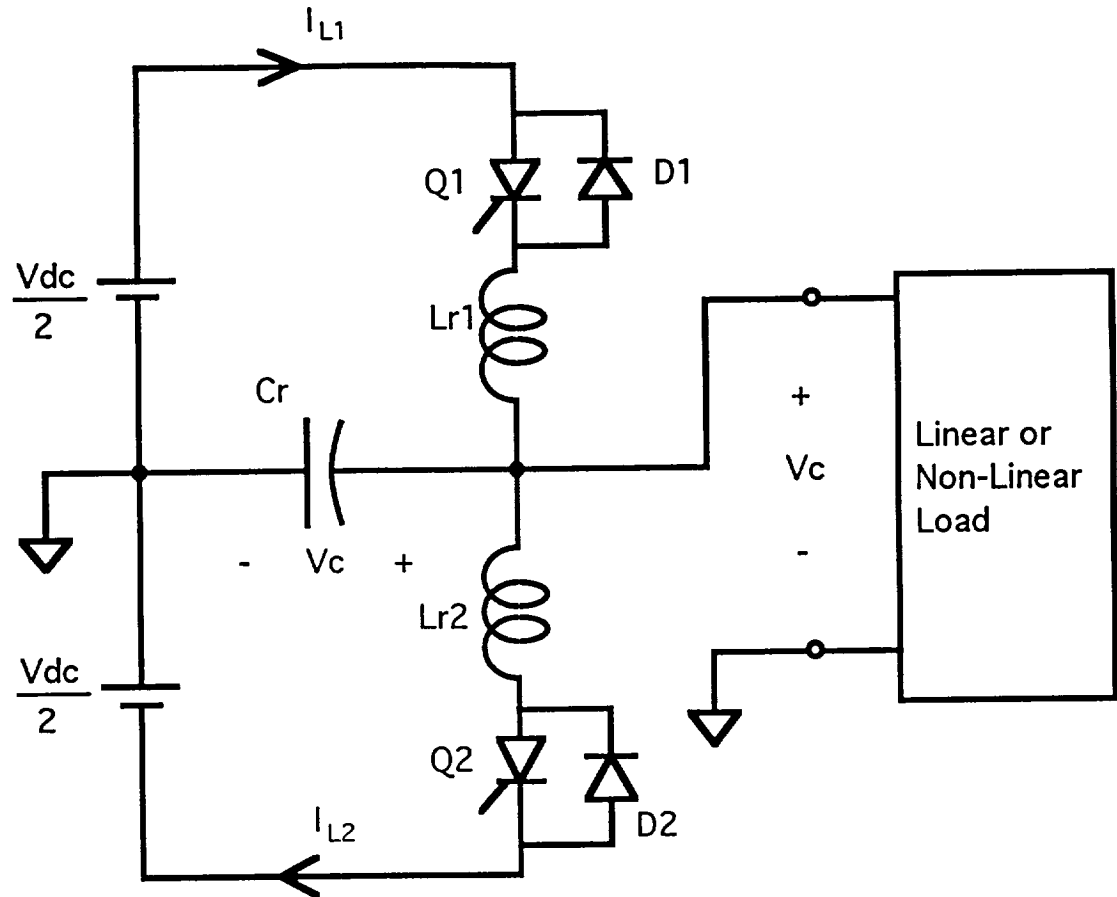


Fig. A3.2 Using a Mapham (resonant) inverter to generate ac voltage.

The analytical expressions for the capacitor voltage and inductor currents are very complicated. However, the waveforms of currents and voltages of this inverter can be obtained by simple qualitative piece-wise linear analysis. At no load, assuming a no-loss case, the positive and negative areas under I_{L1} are equal, thus energy that leaves the battery is same as what goes in. The capacitor current I_C equals to $I_{L1} - I_{L2}$, and its voltage is integral of I_C . The thyristors are switched above the resonant frequency, ω_r , where

$$\omega_r = \frac{1}{\sqrt{L_r C_r}} \quad (\text{A3.1})$$

so that one thyristor will not be fired while the other is still conducting, see the current inductor current waveforms, I_{L1} and I_{L2} , in Fig. A3.3 The resonant frequency is usually

chosen to be around 2/3 of the switching frequency, ω_s . Note that there is sometime when both the inductors are conducting, thus the capacitor sees two inductors in parallel, therefore resonant frequency during that time becomes

$$\omega_r' = \frac{1}{\sqrt{\frac{L_r}{2} C_r}} \quad (\text{A3.2})$$

$$= 1.414 * \omega_r$$

However, it occupies only a small portion of a cycle especially when the inverter is loaded. The current and voltage waveforms of this inverter operated at no load are sketched in Fig. A3.3. Although I_C is a distorted sinewave, the capacitor voltage, V_C , has only small distortion because it is the integral of I_C which smooths out the high frequency components.

Turn-off of the thyristors is a natural commutation process as one thyristor current always crosses zero before the other one is fired. Unfortunately, this inverter has a potential latching problem. If one thyristor is triggered and the other is still carrying current, they will latch on. Under no-load condition or an undamped system, the thyristor turns off at zero current within about $\frac{\pi}{\omega_r}$ seconds. As the inverter is loaded by a resistor, time taken for the current to reach zero becomes to about $\frac{\pi}{\omega_d}$,

where ω_d is called the damped frequency and defined as

$$\omega_d = \omega_r \sqrt{1 - \left(\frac{Z_o}{2R}\right)^2} \quad (\text{A3.3})$$

Z_o is the characteristic impedance,

$$Z_o = \sqrt{\frac{L_r}{C_r}} \quad (\text{A3.4})$$

But the characteristic impedance also change when both inductors are conducting.

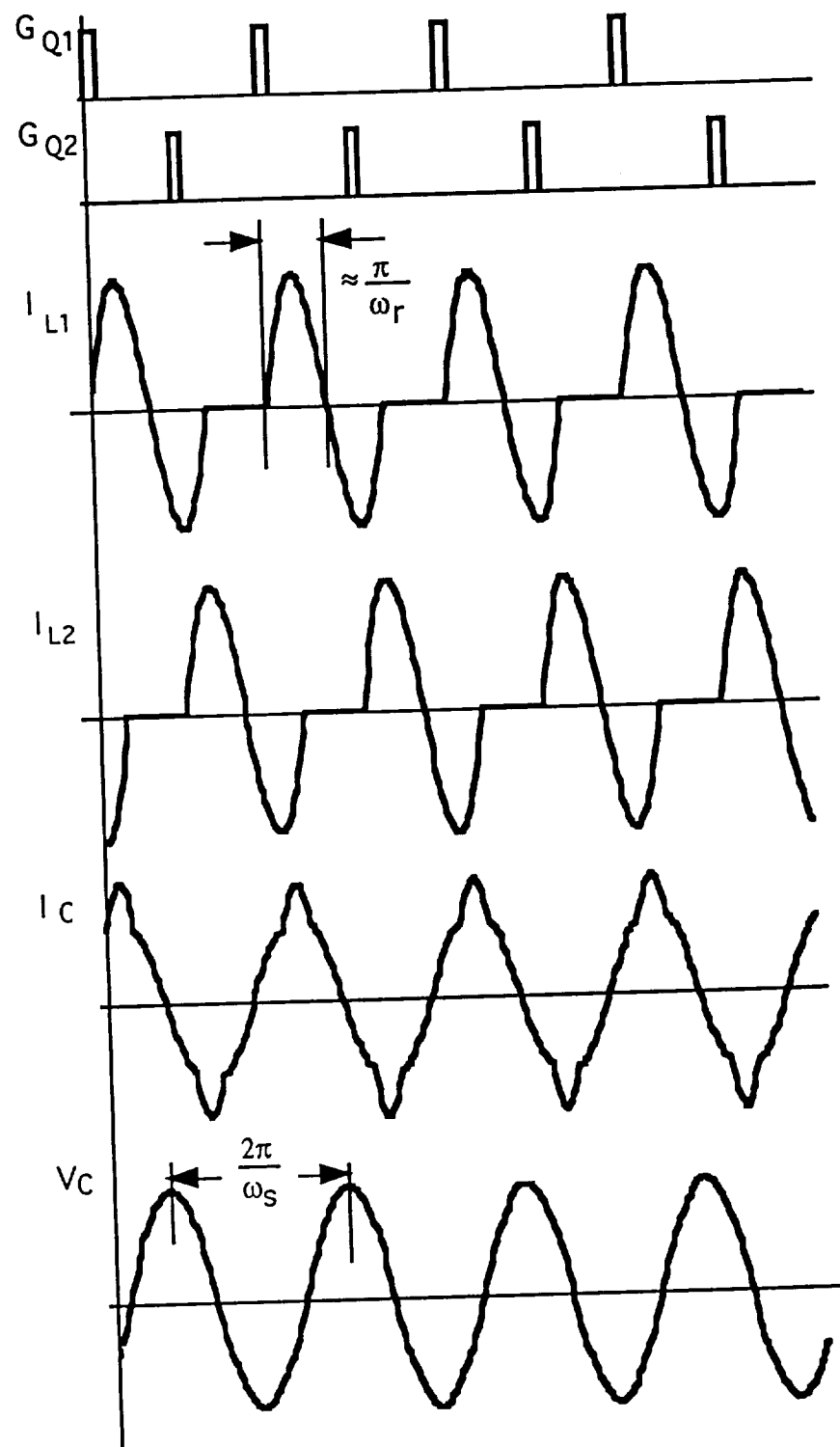


Fig. A3.3 Idealized waveforms of currents and voltage of a Mapham inverter in steady state under no load.

$$Z_o' = \sqrt{\frac{L_r}{2C_r}} = 0.707 * Z_o \quad (A3.5)$$

To avoid this latching problem, the damped frequency, ω_d , should be less than the switching frequency, ω_s , therefore

$$\omega_s < \omega_d \quad (A3.6)$$

For example, if $L_r = 12\mu\text{H}$, $C_r = 3\mu\text{F}$ and $\omega_s = 125,664 \text{ rad/s}$, then, from (A3.3) and (A3.6), R should not be less than 3.1Ω . But if the changes of characteristic impedance, and damped frequency were taken into account R should be slightly bigger. With R equal to 4Ω , simulation of this inverter is shown in Fig. A3.4. The dc voltage, V_{dc} , used in this simulation is 200 V . The peak output voltage, V_C , is 215 V , therefore, this inverter is delivering about 5.5kW . However, in the actual situation this converter cannot deliver that high of power because the turn-off time, t_q , of the thyristors has to be considered. The turn-off time is the time for the thyristor to regain voltage blocking capability. In fact, the turn-off time, t_q , in our case is slightly smaller because the thyristors are naturally commutated.

From the simulation, the negative inductor current last for about $4\mu\text{s}$, which means the thyristor has to block the forward voltage in $4\mu\text{s}$. For a fast thyristor the turn-off time is about $15\mu\text{s}$. With a 10Ω load there is enough time for the device to turn off, see Fig. A3.5. The peak of the output sinewave is $\approx 220\text{V}$, therefore, the power delivered to the 10Ω load is approximately, 2.4kW . As mentioned before, a Mapham inverter has a better voltage regulation than other resonant inverters, from the simulation as shown in Fig. A3.6, the change of voltage from no load to a 10Ω load is only $\approx 5 \text{ V}$ out of 220V .

The efficiency of this converter is quite dependent on how much it is loaded. The more the inverter is loaded the higher the efficiency. As the inverter is loaded, the

negative current, which conducts through the anti-parallel diodes, decreases while the positive current increases only slightly. The reduced current can greatly reduce core and copper losses.

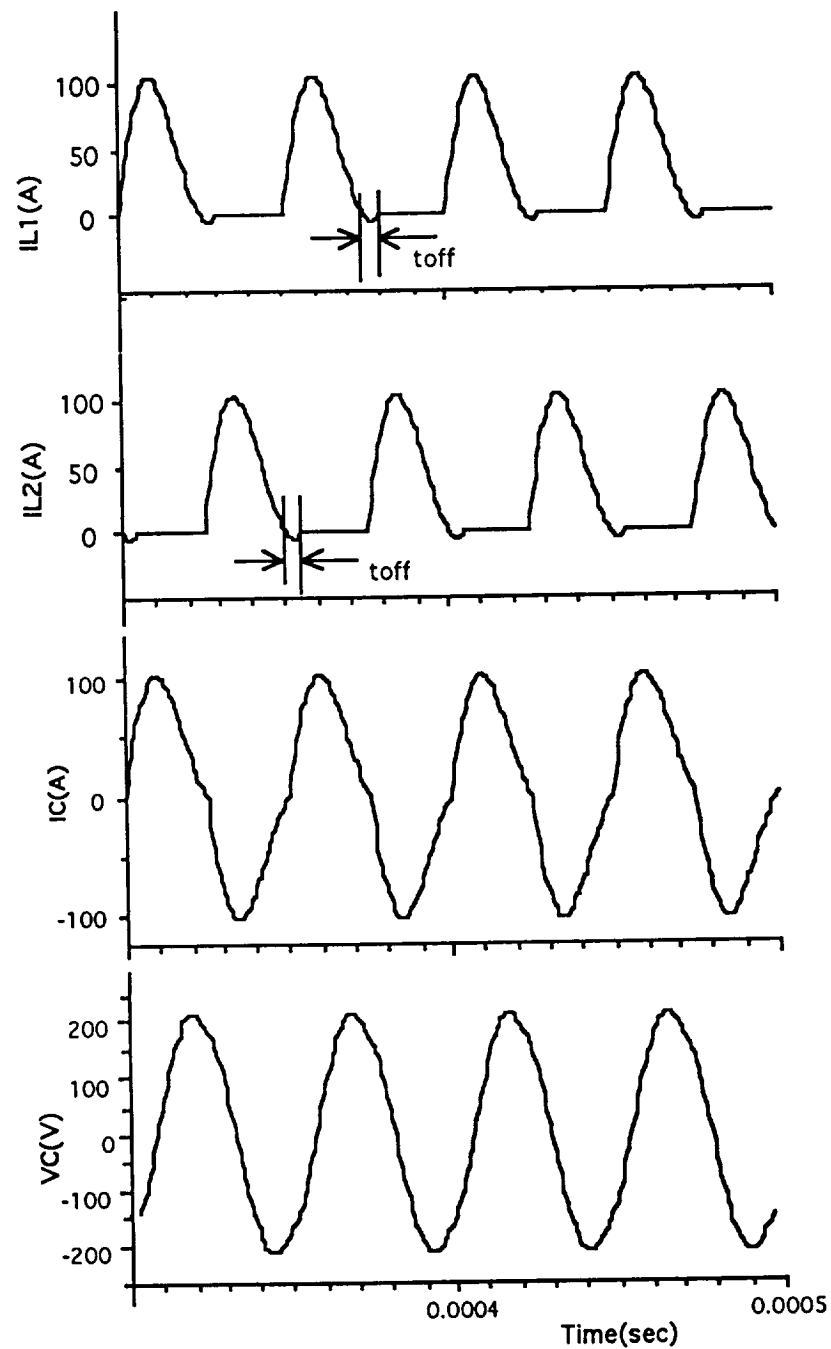


Fig. A3.4 The simulation of a Mapham inverter with a $4\ \Omega$ load connected.

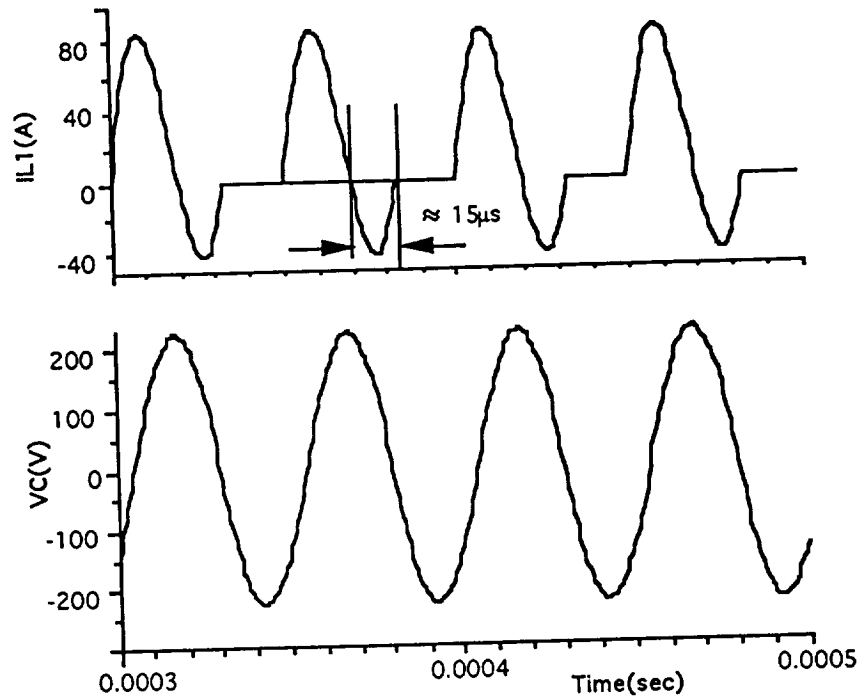


Fig. A3.5 The simulation of a Mapham inverter with a $10\ \Omega$ load connected.

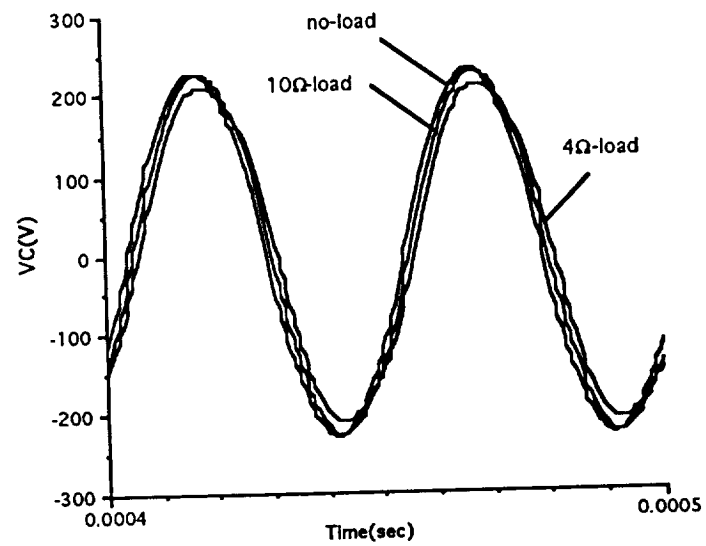


Fig. A3.6 The output voltage regulations at different loads.

The Mapham inverter discussed above can easily drive a linear load with fairly good regulation and negligible distortion. However for a non-linear load, like an ac/ac PDM converter, there is a latching problem even in low power level. From the above analysis, the Mapham inverter can deliver $\approx 2\text{kW}$ to a resistive load, but driving a non-linear load can reduce the maximum power output.

Consider a the single phase current regulated PDM converter loading the Mapham inverter as shown in Fig. A3.7. The output voltage of the PDM converter V_o is filtered by the inductor, L , so that the load current I_R , has less ripple current. In the simulation, L and R are chosen to be 5mH , and 2.5Ω , respectively. The resistor current I_R is regulated to $16 \sin(754 t) \text{ A}$, then the output power is only 320W . From the simulation shown in Fig. A3.8, each time the V_o switches polarity, there is transient inductor current and capacitor voltage between 0.0018s to 0.0026s . During the transient time, as seen in Fig. A3.8(a), the turn-off time for the thyristor can become so small and cause the thyristor re-triggered.

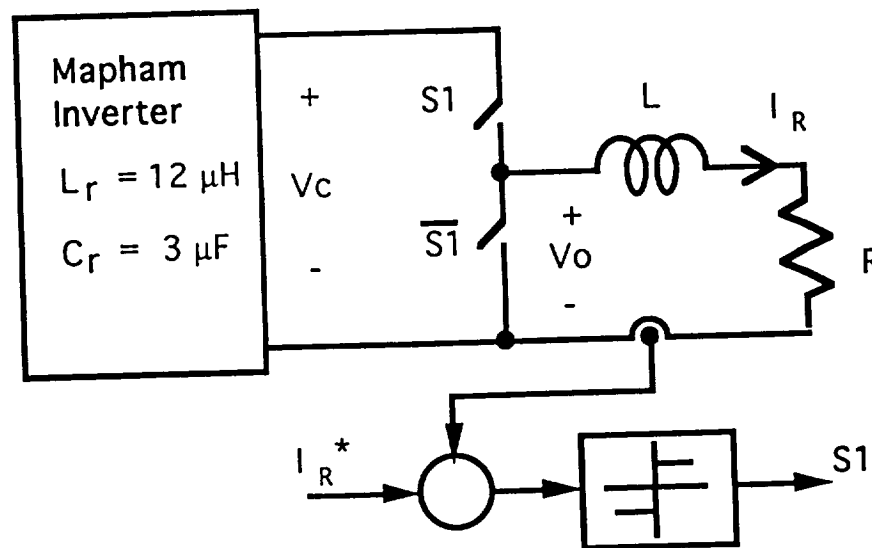


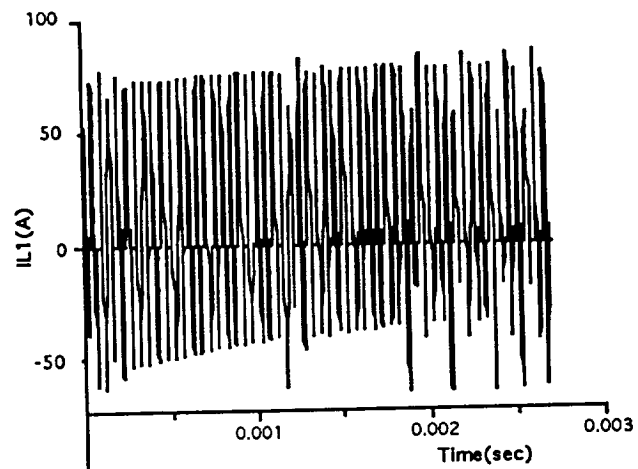
Fig. A3.7 A Mapham inverter loaded by a ac/ac PDM converter.

Moreover, the output voltage of the inverter is not well regulated during that time (Fig. A3.8(b)). Therefore, this "2kW" inverter cannot deliver 320W to a non-linear load like the PDM converter.

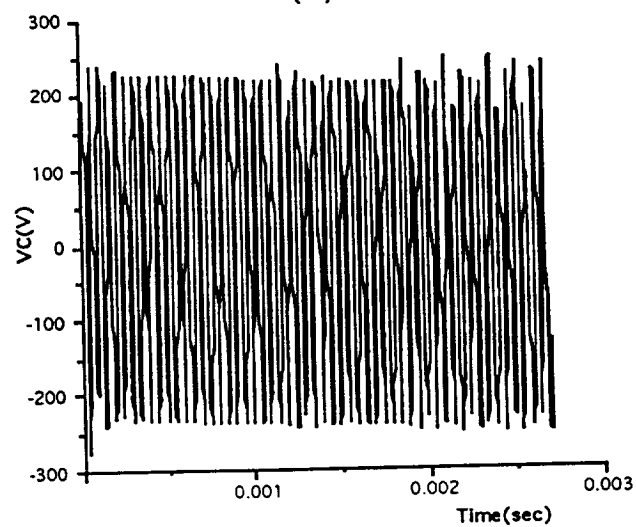
To avoid this latching problem, one can increase the energy size of the resonant tank by decreasing L_r and increasing C_r . By doing that the characteristic impedance decreases and the output voltage of the inverter will be more stiff. However, current and power rating of the thyristors and diodes in the inverter need to be higher. A simulation result with L_r and C_r equal to $6\mu\text{H}$, $6\mu\text{F}$ is shown in Fig. A3.9. The output voltage of the Mapham inverter, Fig. A3.9(b), is better regulated than in Fig. A3.8(b). It can be seen in Fig. A3.9(a), the turn-off time is more consistent and longer compared to that in Fig. A3.8(a).

For the circuit with L_r and C_r equal to $6\mu\text{H}$ and $6\mu\text{F}$, the inductor current is twice as much as the one with L_r and C_r equal to $12\mu\text{H}$, $3\mu\text{F}$, the increased current can also cause high thermal dissipation in the thyristors and latch the devices. Putting thyristors in parallel can spread the inductor current and, therefore, the thermal dissipation, but the size and cost effectiveness of the inverter becomes questionable.

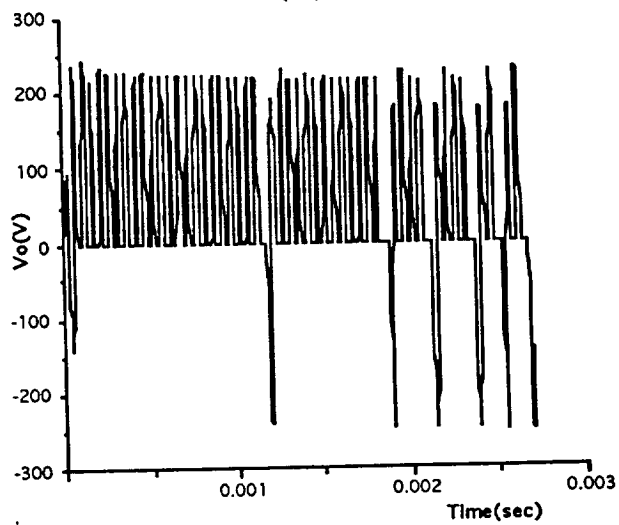
Another kind the non-linear load is shown in Fig. A3.10. This non-linear load does not lower the power rating of the Mapham inverter. In the steady state, the inverter sees a square wave load current with the magnitude of average $\langle V_o \rangle / R$. The load resistor and the filter inductor equal to 10Ω and 2mH respectively. The power output is the same as if a 10Ω load connected to the Mapham inverter directly. The simulation results are shown in Figs. A3.11 and A3.12. Since this load is high impedance, the resonant frequency of the inverter is not affected by the load as in the linear load case mentioned above. The inductor current is equal to the no-load current plus the dc offset I_R (see Fig. A3.11).



(a)

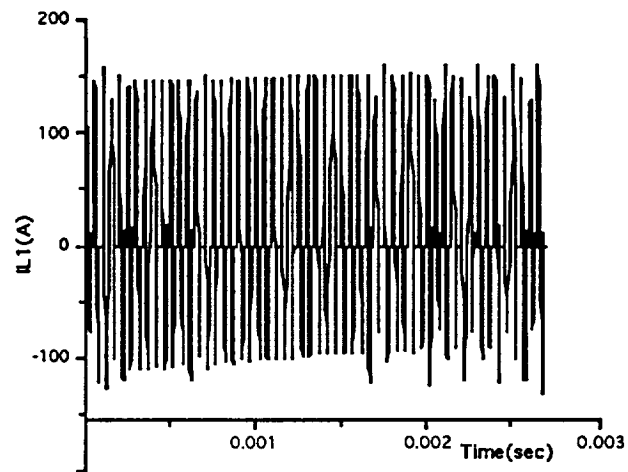


(b)

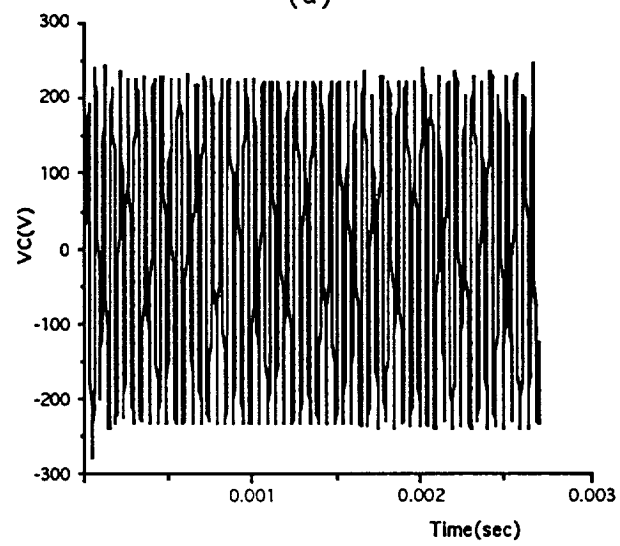


(c)

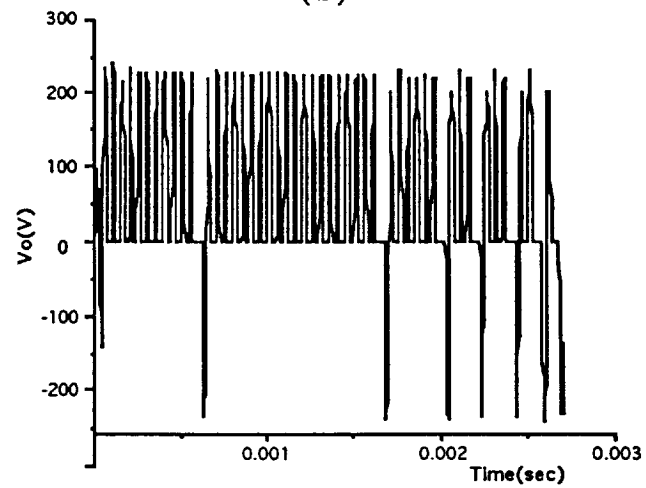
Fig. A3.8 Simulation of the Mapham inverter loaded by a ac/ac PDM converter.



(a)



(b)



(c)

Fig. A3.9 A simulation result with L_r and C_r equal to $6\mu H$, $6\mu F$.

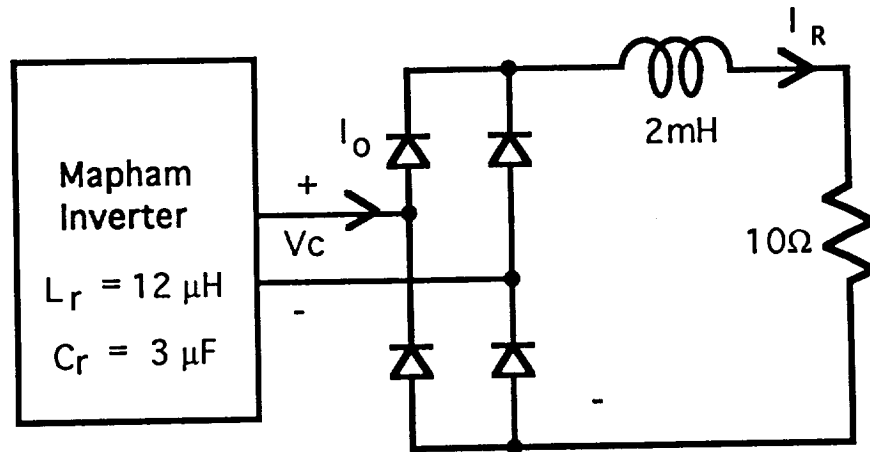


Fig. A3.10 A Mapham Inverter loaded by a full-wave rectifier

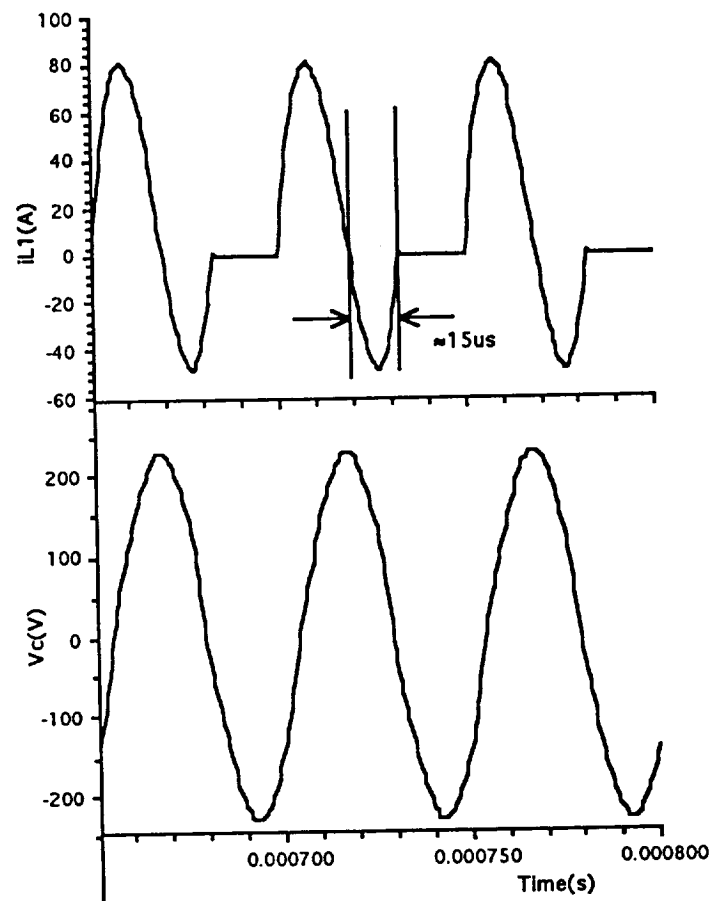


Fig. A3.11 The current of the resonant inductor, L_r , and output voltage of the Mapham inverter shown in Fig. A3.10

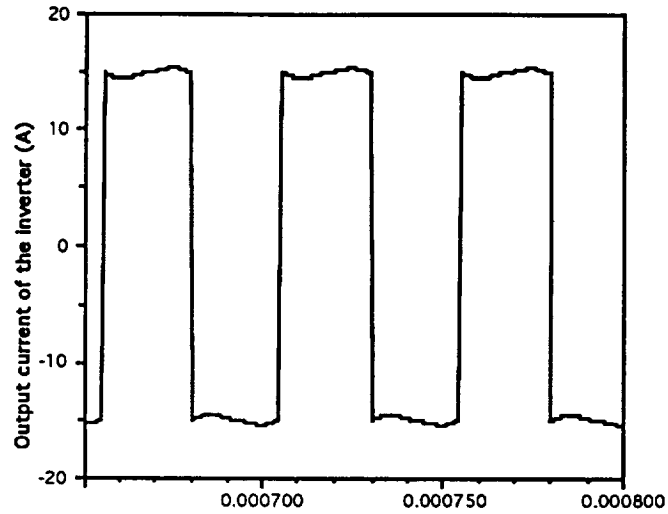


Fig. A3.12 The output current, I_o , of the Mapham inverter in Fig. A3.10.

Although the Mapham inverter used in this research was supposed capable of delivering 2kW, because the PDM converter was a non-linear load, the inverter was not able to provide full power to the PDM converter. The efficiency was estimated to only 40%. With a resistive load of 10 Ω , the efficiency had been measured to $\approx 90\%$.